LECTURE 3. POWER AMPLIFIER DESIGN FUNDAMENTALS

3.1. Main characteristics (two-port networks, gain, delivered power)

3.2. Gain and stability

3.3. Stabilization circuit technique

3.4. Class-A,-B,-C operation modes

3.5. Linearity

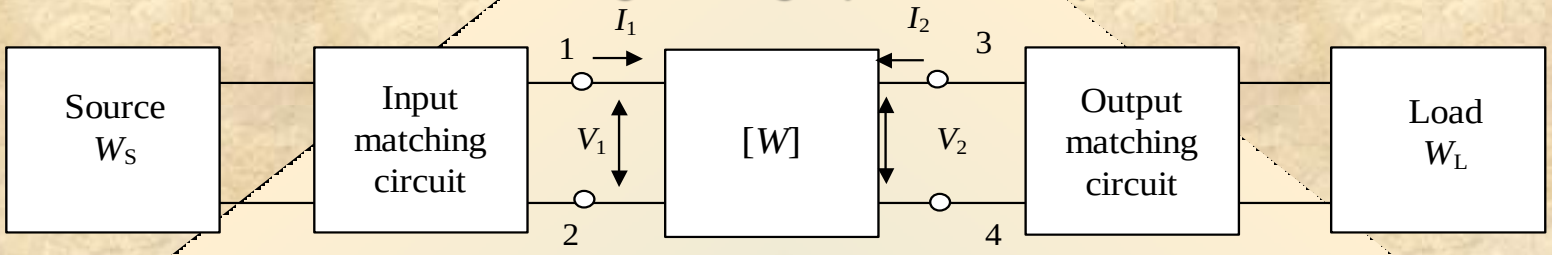
3.6. DC biasing

3.7. Push-pull amplifiers

3.8. Practical aspect of RF and microwave power amplifiers

3.1. Main characteristics

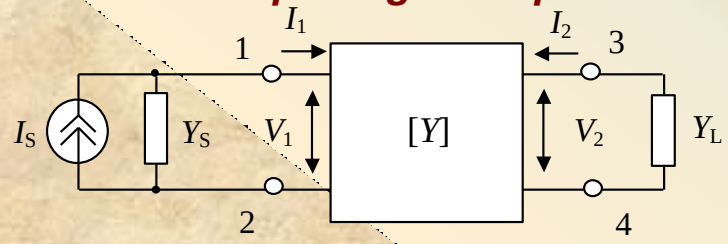
Generalized single-stage power amplifier circuit



Two-port active device is characterized by immitance W-parameters which means system of impedance Z-parameters or admittance Y-parameters

Matching circuits are necessary to transform source W_S and load W_L immitances into definite values between points 1-2 and 3-4, respectively

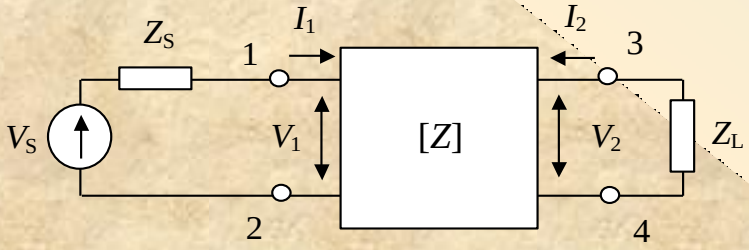
If source of input signal is presented by current source with internal admittance Y_S



⇒ device is characterized by Y-parameters

$$\begin{cases} I_1 = Y_{11}V_1 + Y_{12}V_2 \\ I_2 = Y_{21}V_1 + Y_{22}V_2 \end{cases}$$

If source of input signal is presented by voltage source with internal impedance Z_S



⇒ device is characterized by Z-parameters

$$\begin{cases} V_1 = Z_{11}I_1 + Z_{12}I_2 \\ V_2 = Z_{21}I_1 + Z_{22}I_2 \end{cases}$$

3.1. Main characteristics

Power amplifier gain
(in terms of Y-parameters)

- Operating power gain $G_P = P_L / P_{in}$ - ratio of power dissipated in active load G_L to power delivered to input port of active device with admittance Y_{in} : this gain is independent of G_S but is strongly dependent on G_L

- Available power gain $G_A = P_{out} / P_S$ - ratio of power available at output port of active device with admittance Y_{out} to power available from source G_S : this gain depends on G_S but is independent of G_L

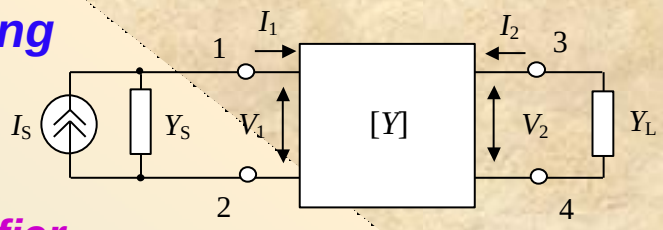
- Transducer power gain $G_T = P_L / P_S$ - ratio of power dissipated in active load G_L to power available from source G_S : this gain strongly depends on both G_S and G_L

- Maximum available gain MAG - theoretical power gain of active device when its reverse transfer function Y_{12} is set equal to zero : represents theoretical gain limit that can be achieved with given device under assumption of conjugate input and output impedance matching

3.1. Main characteristics

Operating power gain

Two types of power gain are widely used: operating power gain G_P and transducer power gain G_T



- **operating power gain to characterize device amplifying capability and multistage power amplifier**
- **transducer power gain to evaluate input matching and stability**

Power flowing from input port

$$P_{\text{in}} = 0.5 V_1^2 \operatorname{Re} Y_{\text{in}}$$

From

$$\begin{cases} I_1 = Y_{11} V_1 + Y_{12} V_2 \\ I_2 = Y_{21} V_1 + Y_{22} V_2 \end{cases}$$

in view of $I_2 = -Y_{\text{L}} V_2$

→ **input admittance**

$$Y_{\text{in}} = \frac{I_1}{V_1} = Y_{11} - \frac{Y_{12} Y_{21}}{Y_{22} + Y_{\text{L}}}$$

Output power dissipated in load

$$P_{\text{L}} = 0.5 V_2^2 \operatorname{Re} Y_{\text{L}}$$

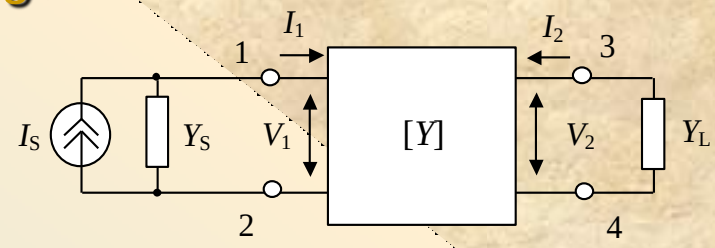
→ **operating power gain**

$$G_{\text{P}} = \frac{P_{\text{L}}}{P_{\text{in}}} = \frac{\left| Y_{21} \right|^2 \operatorname{Re} Y_{\text{L}}}{\left| Y_{22} + Y_{\text{L}} \right|^2 \operatorname{Re} Y_{\text{in}}}$$

3.1. Main characteristics

Transducer power gain

Transducer power gain G_T includes assumption of conjugate matching both load and source



Power flowing from input port

$$P_S = \frac{I_S^2}{8\,\mathrm{Re}\,Y_S}$$

From

$$\begin{cases} I_1 = Y_{11}V_1 + Y_{12}V_2 \\ I_2 = Y_{21}V_1 + Y_{22}V_2 \end{cases}$$

in view of

$$I_S = Y_S V_1 + I_1$$

→ **source current**

$$I_S = \frac{(Y_{11} + Y_S)(Y_{22} + Y_L) - Y_{12}Y_{21}}{Y_{22} + Y_L} V_1$$

Output power dissipated in load

$$P_L = 0.5 V_2^2 \,\mathrm{Re}\, Y_L$$

→ **transducer power gain**

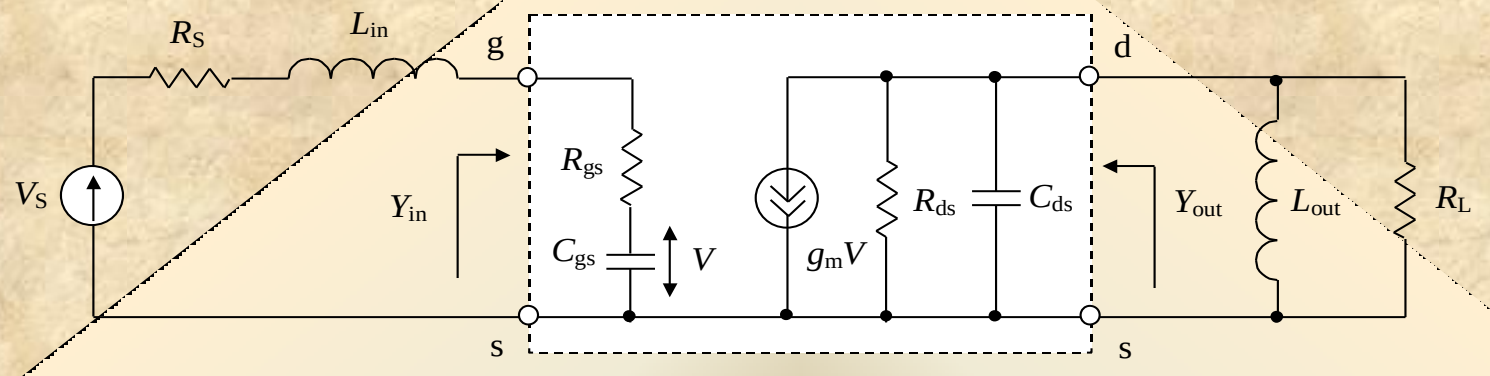
$$G_T = \frac{P_L}{P_S} = \frac{4\left|Y_{21}\right|^2 \mathrm{Re}Y_S\, \mathrm{Re}Y_L}{\left|(Y_{11} + Y_S)(Y_{22} + Y_L) - Y_{12}Y_{21}\right|^2}$$

Maximum available gain
($Y_{12} = 0$, $Y_S = Y_{11}^*$, $Y_L = Y_{22}^*$)

$$MAG = \frac{\left|Y_{21}\right|^2}{4\,\mathrm{Re}Y_{11}\mathrm{Re}Y_{22}}$$

3.1. Main characteristics

Small-signal FET power amplifier



Equivalent circuit with $C_{gd} = 0$

$$Y_{11} = j\omega C_{gs} / (1 + j\omega R_{gs} C_{gs})$$

$$Y_{12} = 0$$

$$Y_{21} = g_m / (1 + j\omega R_{gs} C_{gs})$$

$$Y_{22} = (1/R_{ds}) + j\omega C_{ds}$$

$$G_T(f) = G_T(f_T)\left(\frac{f_T}{f}\right)^2$$

- gain estimation at any frequency vs gain at transition frequency

Input and output conjugate matching

$$R_S = R_{gs} \qquad R_L = R_{ds}$$

$$L_{in} = 1/\omega^2 C_{gs} \qquad L_{out} = 1/\omega^2 C_{ds}$$

$$G_T(C_{gd} = 0) = MAG = \left(\frac{f_T}{f}\right)^2 \frac{R_{ds}}{4R_{gs}}$$

$$f_T = g_m / 2\pi C_{gs}$$ **- transition frequency**

$$f_{max} = \frac{f_T}{2}\sqrt{\frac{R_{ds}}{R_{gs}}}$$ **- maximum frequency where MAG = 1**

3.2. Gain and stability

Principle of power amplifier design - to provide maximum power gain and efficiency for given output power with predictable degree of stability

Main reasons of instability:

- ***positive feedback from output to input through intrinsic feedback capacitance or inductance of common-grounded terminal***
- ***oscillation conditions due to external elements forming positive feedback loop***

In terms of immitance approach, circuit will be unconditionally stable if for both hypothetical conditions of open-circuited input and output ports:

$$\begin{cases} \mathrm{Re}\left[W_S(\omega)+W_{in}(\omega)\right] > 0 \\ \mathrm{Im}\left[W_S(\omega)+W_{in}(\omega)\right] = 0 \end{cases} \qquad \begin{cases} \mathrm{Re}\left[W_L(\omega)+W_{out}(\omega)\right] > 0 \\ \mathrm{Im}\left[W_L(\omega)+W_{out}(\omega)\right] = 0 \end{cases}$$

In case of opposite signs, active two-port network can be treated as unstable or potentially unstable (having negative input or output immitance)

When $\mathrm{Re}\left[W_S(\omega)\right] > 0$ $\mathrm{Re}\left[W_L(\omega)\right] > 0$

Requirements of power amplifier stability can be simplified to

$$\mathrm{Re}\left[W_{in}(\omega)\right] > 0 \quad \mathrm{Re}\left[W_{out}(\omega)\right] > 0$$

3.2. Gain and stability

Device stability

In common case, value of ReW_{out} depends on W_S $\Rightarrow$ within definite values of W_S, $ReW_{out} < 0$ and two-port network will be potentially unstable

$$W_{out} = W_{22} - \frac{W_{12}W_{21}}{W_{11} + W_S}$$

To provide unconditional stability $\quad \mathrm{Re}\left[W_{out}(\omega)\right]\big|_{min} > 0$

$$\partial\, \mathrm{Re}W_{out} / \partial\, \mathrm{Im}W_S = 0 \quad \Rightarrow \quad \mathrm{Re}W_{out} = \mathrm{Re}W_{22} - \frac{\left|W_{12}W_{21}\right| + \mathrm{Re}\left(W_{12}W_{21}\right)}{2\mathrm{Re}\left(W_{11} + W_S\right)}$$

Minimum positive value when $ReW_S = 0$:

$$\mathrm{Re}W_{out} = \mathrm{Re}W_{22} - \frac{\left|W_{12}W_{21}\right| + \mathrm{Re}\left(W_{12}W_{21}\right)}{2\mathrm{Re}\left(W_{11}\right)}$$

$$2\mathrm{Re}W_{11}\,\mathrm{Re}W_{22} - \left|W_{12}W_{21}\right| - \mathrm{Re}\left(W_{12}W_{21}\right) > 0$$

$$K = \frac{2\,\mathrm{Re}W_{11}\,\mathrm{Re}W_{22} - \mathrm{Re}\left(W_{12}W_{21}\right)}{\left|W_{12}W_{21}\right|}$$

- device stability factor

Unconditional stability: $K > 1$

Potential instability: $-1 < K < 1$

3.2. Gain and stability

Circuit stability

When active device is potentially unstable, power amplifier stability can be improved with proper choice of source and load immitances, W_S and W_L:

$$K_T = \frac{2\,\mathrm{Re}\left(W_{11} + W_S\right)\mathrm{Re}\left(W_{22} + W_L\right) - \mathrm{Re}\left(W_{12}W_{21}\right)}{\left|W_{12}W_{21}\right|} > 1$$

Maximum gain with unconditionally stable device

When K > 1, it is necessary to choose load immitance W_L to maximize finite value of operating power gain G_P :

$$G_P = \frac{P_L}{P_{in}} = \frac{\left|W_{21}\right|^2 \mathrm{Re}W_L}{\left|W_{22} + W_L\right|^2 \mathrm{Re}W_{in}}$$

$$\frac{\partial G_P}{\partial\,\mathrm{Re}W_L} = 0$$

$$\frac{\partial G_P}{\partial\,\mathrm{Im}W_L} = 0$$

$$\mathrm{Re}W_L^o = \frac{\left|W_{12}W_{21}\right|}{2\mathrm{Re}W_{11}}\sqrt{K^2 - 1}$$

$$\mathrm{Im}W_L^o = \frac{\mathrm{Im}\left(W_{12}W_{21}\right)}{2\mathrm{Re}W_{11}} - \mathrm{Im}W_{22}$$

$$G_{Pmax} = \left|\frac{W_{21}}{W_{12}}\right| / \left(K + \sqrt{K^2 - 1}\right)$$

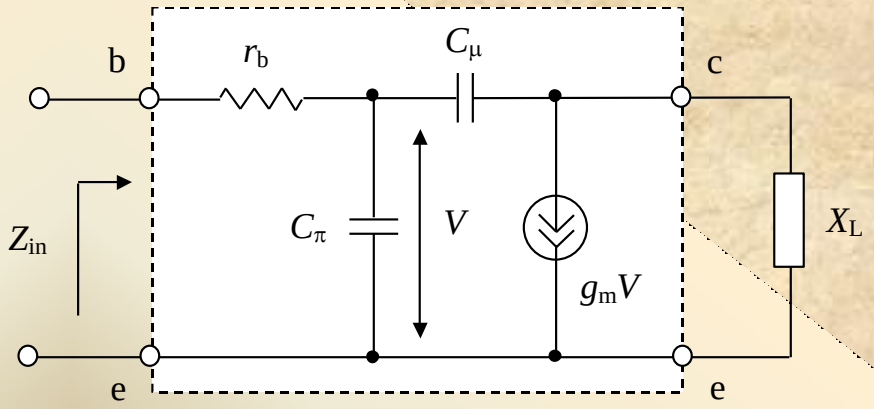
- maximum gain (maximum achievable value at K = 1)

3.3. Stabilization circuit technique

Frequency domains of BJT potential instability

Stability factor through Z-parameters:

$$K = \frac{2R_{11}R_{22} - \mathrm{Re}(Z_{12}Z_{21})}{|Z_{12}Z_{21}|}$$



BJT equivalent circuit Z-parameters:

$$Z_{11} = r_b + \frac{1}{g_m} / \left(1 + j\frac{\omega}{\omega_T}\right)$$

$$Z_{12} = \frac{1}{g_m} / \left(1 + j\frac{\omega}{\omega_T}\right)$$

$$Z_{21} = \left(\frac{1}{g_m} - \frac{1}{j\omega C_\mu}\right) / \left(1 + j\frac{\omega}{\omega_T}\right)$$

$$Z_{22} = \left(\frac{1}{g_m} + \frac{1}{\omega_T C_\mu}\right) / \left(1 + j\frac{\omega}{\omega_T}\right)$$

BJT stability factor

$$K = 2r_b g_m \frac{1 + \frac{g_m}{\omega_T C_\mu}}{\sqrt{1 + \left(\frac{g_m}{\omega C_\mu}\right)^2}}$$

Maximum value at higher frequencies:

$$K = 2r_b g_m \left(1 + \frac{g_m}{\omega_T C_\mu}\right)$$

3.3. Stabilization circuit technique

Frequency domains of BJT potential instability

At low frequencies if to take into account dynamic base-emitter resistance r_π and Early collector-emitter resistance r_0 $\Rightarrow$ K > 1

Only one unstable frequency domain with low f_{p1} and high f_{p2} boundary frequencies

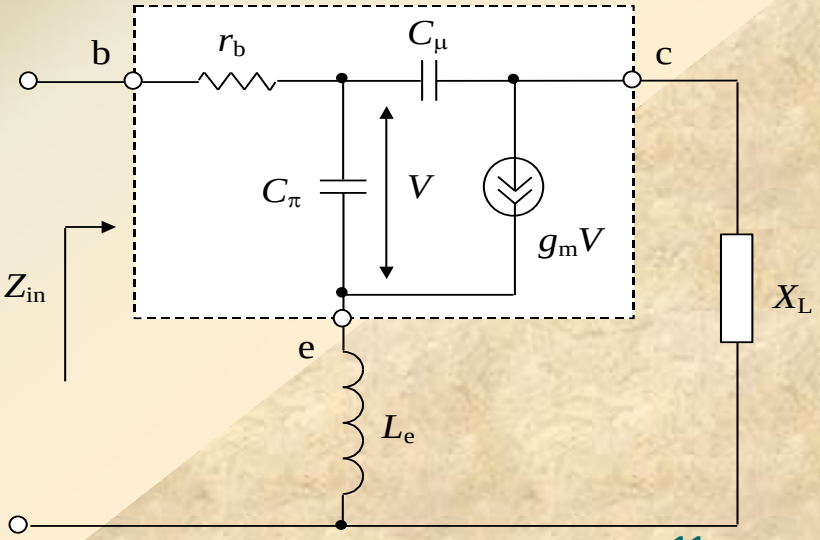
For K = 1 $$f_{p2} = \frac{g_m}{2\pi C_\mu} \Big/ \sqrt{(2 r_b g_m)^2 \left(1 + \frac{g_m}{\omega_T C_\mu}\right)^2 - 1}$$ **or** $$f_{p2} \cong \frac{1}{4\pi r_b C_\pi}$$

In common case, at higher frequencies with parasitic emitter lead inductance L_e :

Expression for low f_{p3} and high f_{p4} boundary frequencies of second domain of BJT potential instability

$$f_{p3,4} = f_T \sqrt{\frac{1 - 4\omega_T r_b C_\mu}{8\omega_T r_b C_\mu} \mp \sqrt{\left(\frac{1 - 4\omega_T r_b C_\mu}{8\omega_T r_b C_\mu}\right)^2 - \frac{1 + \kappa}{\omega_T r_b C_\mu \kappa^2}}}$$

where $$\kappa = \omega_T L_e / r_b$$



3.3. Stabilization circuit technique

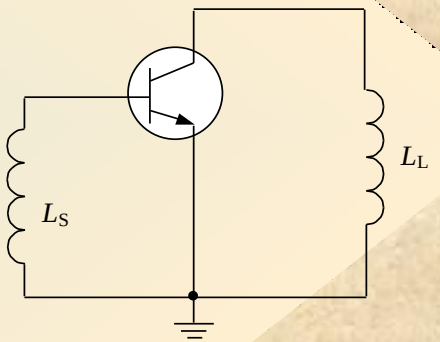
Frequency domains of BJT potential instability

Appearance of second frequency domain of BJT potential instability is result of simultaneous effect of feedback capacitance C_μ and emitter lead inductance L_e

- **first case for $L_e = 0$ and reactive load X_L: one frequency domain of potential instability**

Hartley oscillator

$$Z_{in} = r_b + \frac{1}{g_m} \cdot \frac{1}{1 + j\frac{\omega}{\omega_T}} \cdot \frac{1 + \frac{g_m}{\omega C_\mu}}{1 + \frac{g_m}{\omega_T C_\mu}\left(1 - \omega C_\mu X_L\right) + j g_m X_L}$$



Boundary condition of first potential instability domain:

$$\frac{L_L}{L_S} \approx \frac{1}{\omega_T r_b C_\mu}$$

to prevent oscillations $\Rightarrow$ reduce value of collector choke inductance and increase value of base choke inductance

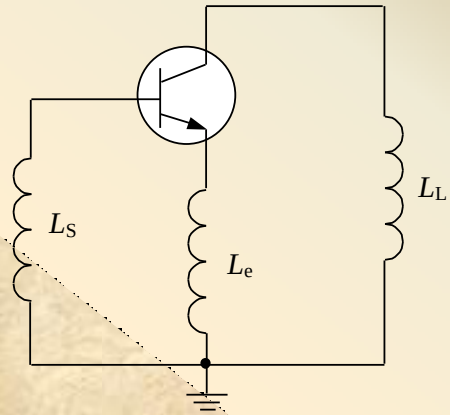
3.3. Stabilization circuit technique

Frequency domains of BJT potential instability

Appearance of second frequency domain of BJT potential instability is result of simultaneous effect of feedback capacitance C_μ and emitter lead inductance L_e

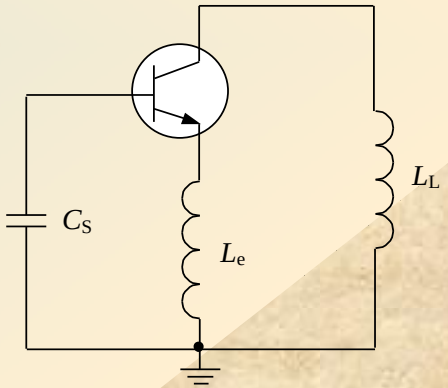
- **second case for $L_e \neq 0$ and reactive load X_L: two frequency domains of potential instability**

first frequency domain



- parasitic oscillator with inductive source and load reactances

second frequency domain



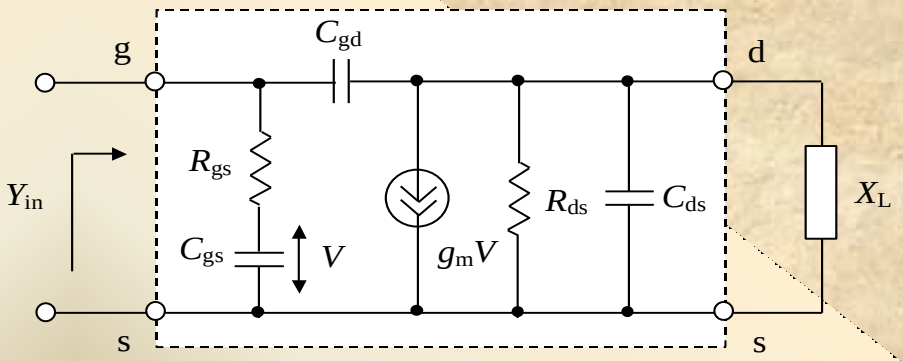
- parasitic oscillator with capacitive source and inductive load reactances

3.3. Stabilization circuit technique

Frequency domains of MOSFET potential instability

Stability factor through Y-parameters:

$$K = \frac{2\,G_{11}G_{22} - \mathrm{Re}\left(G_{12}G_{21}\right)}{\left|Y_{12}Y_{21}\right|}$$



MOSFET equivalent circuit Y-parameters:

$$Y_{11} = \frac{j\omega C_{gs}}{1 + j\omega R_{gs}C_{gs}} + j\omega C_{gd}$$

$$Y_{12} = -j\omega C_{gd}$$

$$Y_{21} = \frac{g_m}{1 + j\omega R_{gs}C_{gs}} - j\omega C_{gd}$$

$$Y_{22} = \frac{1}{R_{ds}} + j\omega\left(C_{ds} + C_{gd}\right)$$

MOSFET stability factor:

$$K = \left[1 + \frac{2}{g_m R_{ds}}\left(1 + \frac{C_{gs}}{C_{gd}}\right)\right]\frac{\omega R_{gs}C_{gs}}{\sqrt{1 + \left(\omega R_{gs}C_{gs}\right)^2}}$$

Maximum value at higher frequencies:

$$K = \left[1 + \frac{2}{g_m R_{ds}}\left(1 + \frac{C_{gs}}{C_{gd}}\right)\right]$$

3.3. Stabilization circuit technique

Frequency domains of MOSFET potential instability

At low frequencies if to take into account gate leakage resistance ⇒ K > 1

Only one unstable frequency domain with low f_{p1} and high f_{p2} boundary frequencies

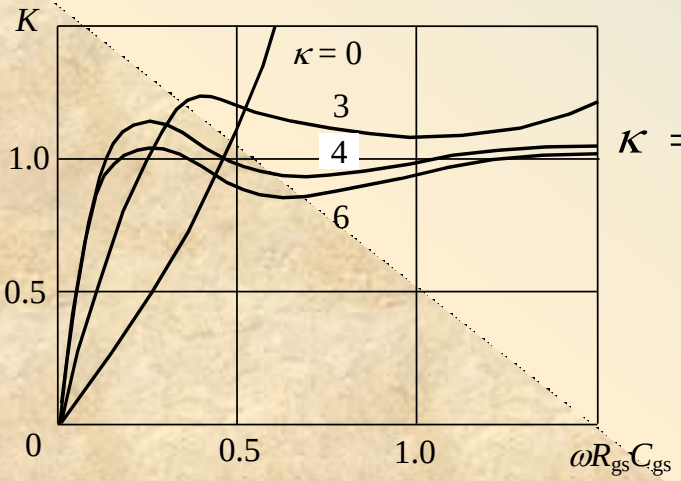
For K = 1

$$f_{p2} = \frac{1}{4\pi R_{gs} C_{gs}} \cdot \frac{g_m R_{ds}}{\sqrt{1 + \frac{C_{gs}}{C_{gd}}}} \cdot \frac{1}{\sqrt{1 + \frac{C_{gs}}{C_{gd}} + g_m R_{ds}}}$$

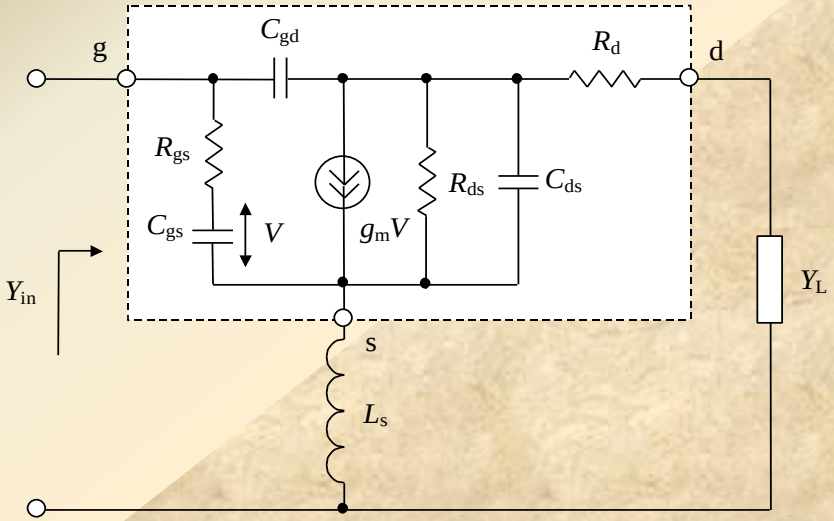
or

$$f_{p2} \approx \frac{1}{4\pi R_{gs} C_{gs}}$$

In common case, parasitic emitter lead inductance L_e creates second frequency domain of potential instability at higher frequencies



$$\kappa = \omega_T L_s / R_{gs}$$



When κ = 3.5 ⇒ second frequency domain disappears

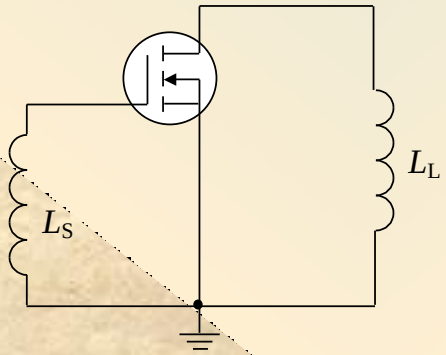
3.3. Stabilization circuit technique

Frequency domains of MOSFET potential instability

Appearance of second frequency domain of MOSFET potential instability is result of simultaneous effect of feedback capacitance C_{gd} and source lead inductance L_s

- **first case for $L_S = 0$ and reactive load X_L: one frequency domain of potential instability**

$$Y_{in} = \frac{j\omega C_{gs}}{1 + j\omega R_{gs} C_{gs}} \left[1 + g_m R_{ds} \frac{1 - j\frac{\omega}{\omega_T}\left(1 + j\omega R_{gs} C_{gs}\right)}{1 + j\omega R_{ds} C_{ds}\left(1 + \frac{C_{gd}}{C_{ds}} + \frac{B_L}{\omega C_{ds}}\right)} \right]$$



Hartley oscillator

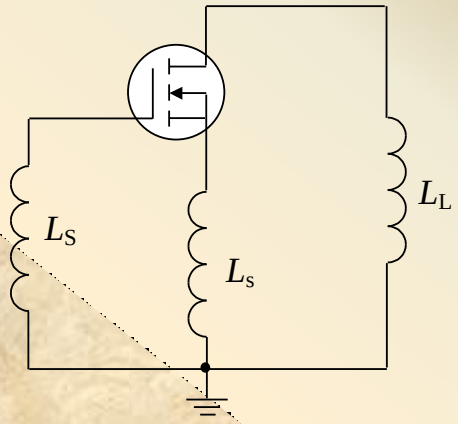
3.3. Stabilization circuit technique

Frequency domains of MOSFET potential instability

Appearance of second frequency domain of MOSFET potential instability is result of simultaneous effect of feedback capacitance C_{gd} and source lead inductance L_s

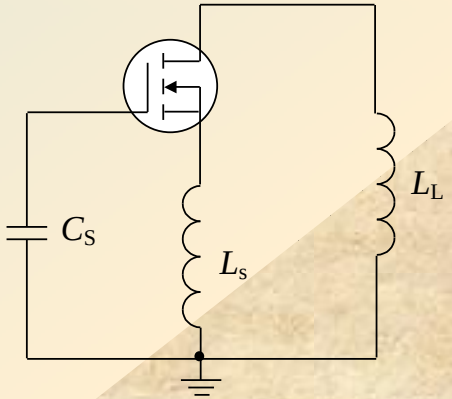
- **second case for $L_S \neq 0$ and reactive load X_L: two frequency domain of potential instability**

first frequency domain



- parasitic oscillator with inductive source and load reactances

second frequency domain



- parasitic oscillator with capacitive source and inductive load reactances

3.3. Stabilization circuit technique

General requirements to provide stable operation of power amplifier:

- ***use active device with stability factor K > 1***

- ***if it is impossible to choose active device with K > 1, provide circuit stability factor K_T > 1 on operating frequency by appropriate choice of real parts of source and load immitances***

- ***disrupt equivalent circuit of possible parasitic oscillators***

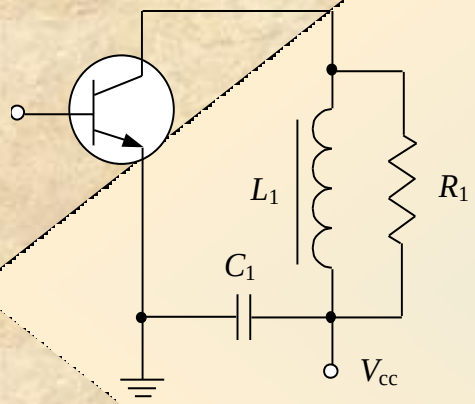
- ***choose such reactive parameters of matching circuits adjacent to input and output of active device which are necessary to avoid self-oscillation conditions***

In common case, it is difficult to propose unified approach to provide stable operation of different power amplifiers especially for multistage power amplifier

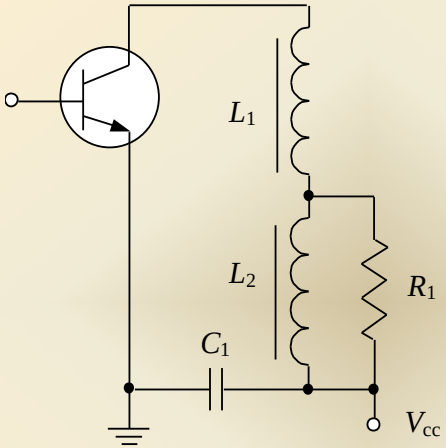
3.3. Stabilization circuit technique

Stability analysis must be done in different frequencies ranges:

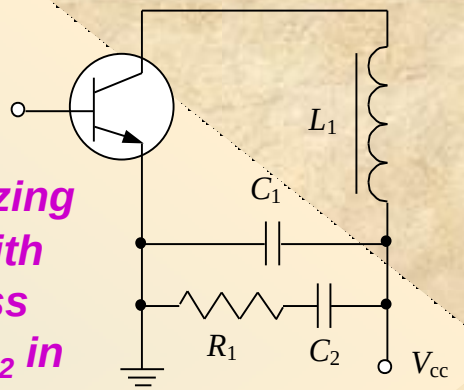
- **at lower frequencies when frequency of parasitic oscillations f_p is significantly smaller operating frequency f_0 ($f_p << f_0$)**



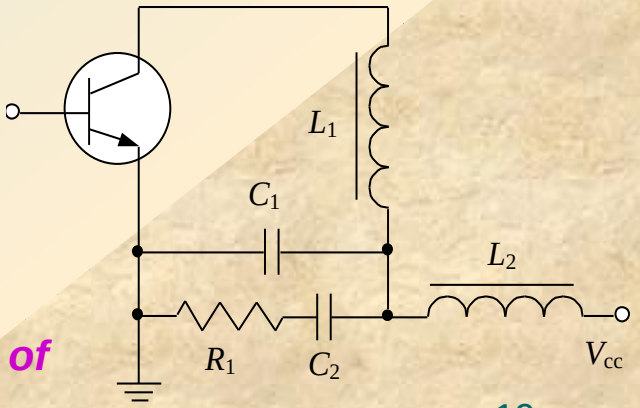
- using stabilizing resistor R_1 in parallel to RF choke



- using stabilizing resistor R_1 in parallel to additional RF choke to avoid degradation of RF performance



- using stabilizing resistor R_1 with series bypass capacitance C_2 in parallel to power supply

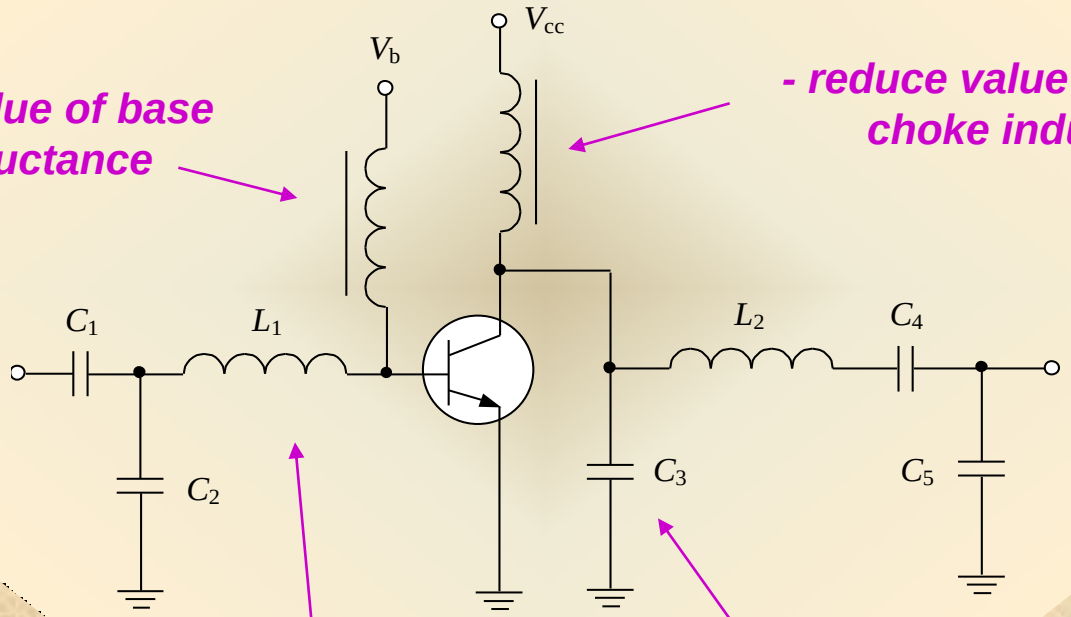


- using additional RF choke if impedance of series R_1C_2 circuit is too high

3.3. Stabilization circuit technique

Stability analysis must be done in different frequencies ranges:

- **at higher frequencies when frequency of parasitic oscillations f_p is significantly higher operating frequency f_0 ($f_p >> f_0$)**



- increase value of base choke inductance

- reduce value of collector choke inductance

- inductive impedance at device input

- capacitive impedance at device output

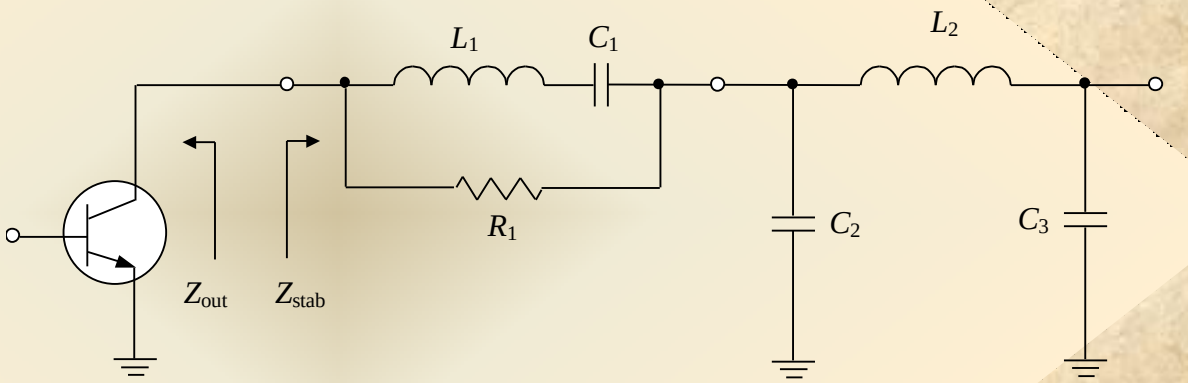
3.3. Stabilization circuit technique

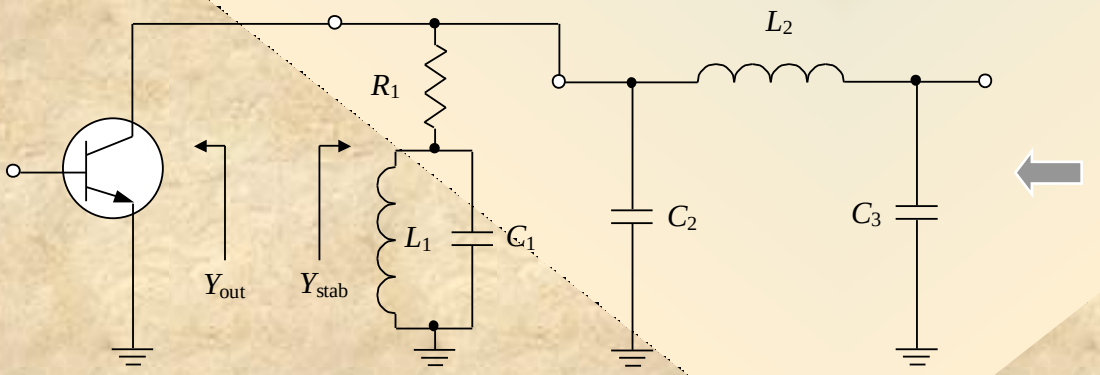
Stability analysis must be done in different frequencies ranges:

- **near operating frequency frequency when frequency of parasitic oscillations f_p is close to operating frequency f_0 ($f_p \approx f_0$)**

series connection of stabilizing RLC circuit connected in series between active device and output matching circuit

series L_1C_1 circuit is tuned on operating frequency

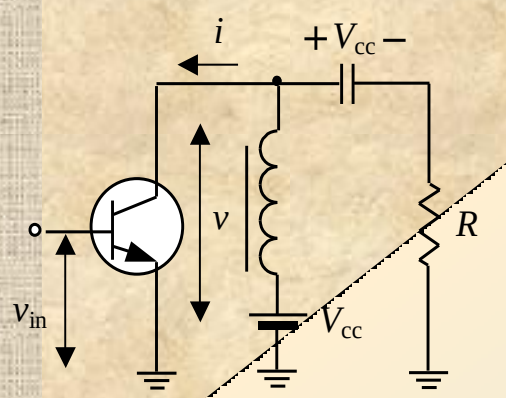




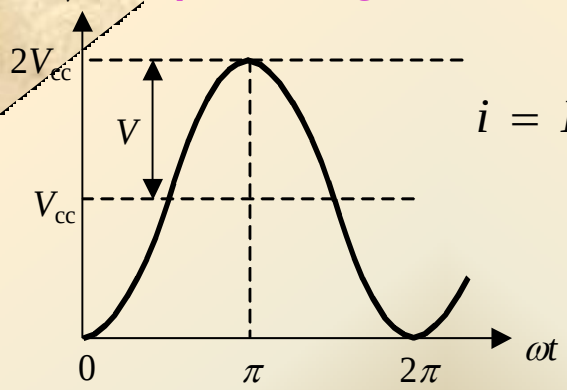
parallel connection of stabilizing RLC circuit between active device and output matching circuit

3.4. Class-A,-B,-C operation modes

Class A



Output voltage



$$v_{in} = V_b + V_{in}\cos\omega t$$

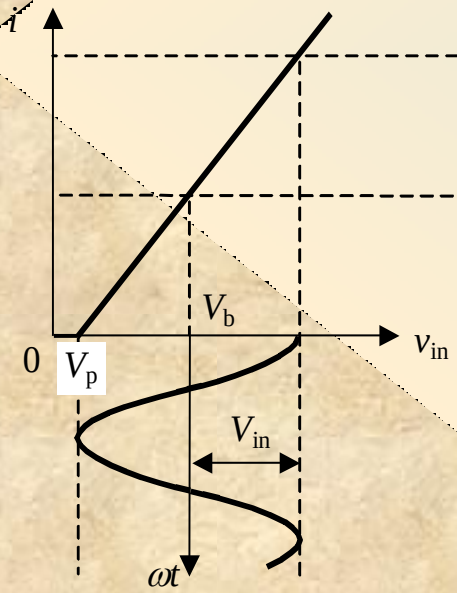
- input cosinusoidal voltage

$$i = I_q + I\cos\omega t$$ ***- output cosinusoidal current***

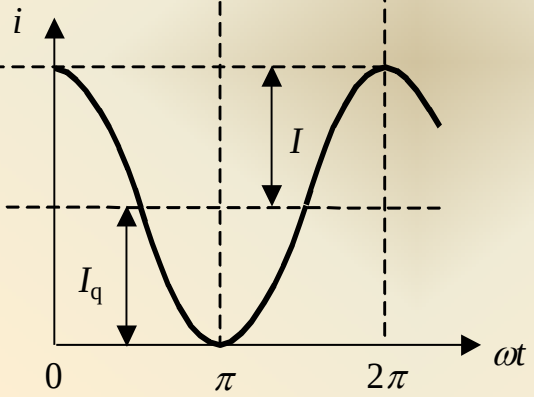
$$v = V_{cc} - V\cos\omega t$$

- output cosinusoidal current

Transfer characteristic



Input voltage



Output current

$$P_0 = I_q V_{cc}$$ ***- DC output power***

$$P = 0.5\,I\,V$$ ***- fundamental output power***

$$\eta = \frac{P}{P_0} = \frac{1}{2}\frac{I}{I_q}\frac{V}{V_{cc}} = \frac{1}{2}\frac{I}{I_q}\xi$$

- collector efficiency

$$\xi = V / V_{cc}$$ ***- voltage peak factor***

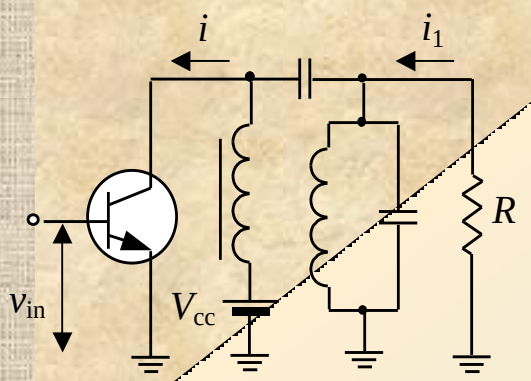
For ideal condition of zero saturation voltage when

$$I / I_q = 1$$
$$\xi = 1$$

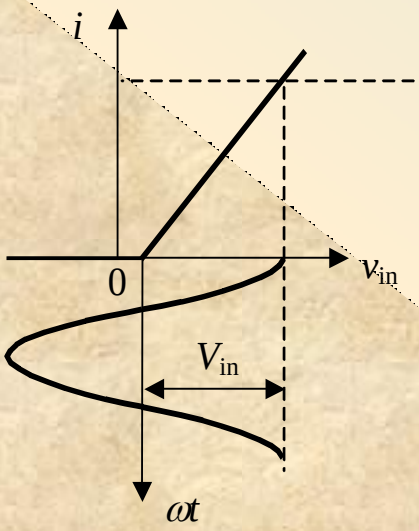
$$\eta = 0.5$$ ***- maximum collector efficiency in Class A***

3.4. Class-A,-B,-C operation modes

Class B

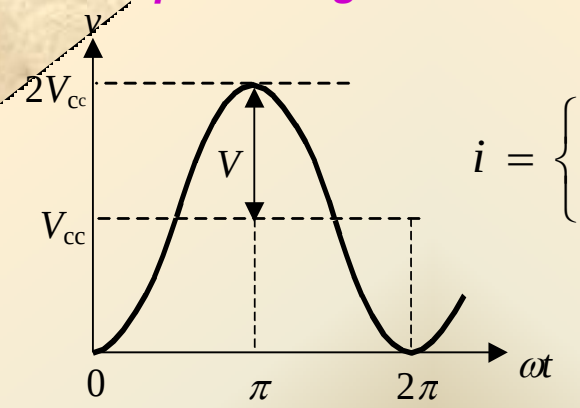


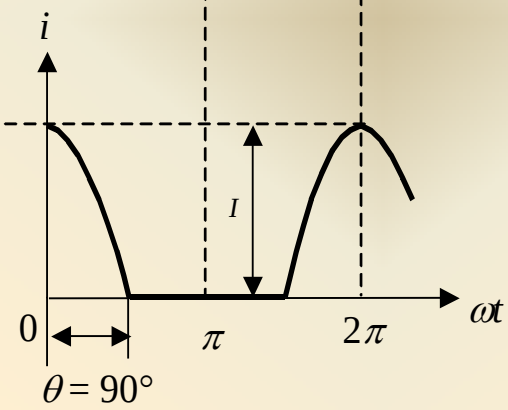
Transfer characteristic



Input voltage

Output voltage





Output current

$$v_{in} = V_b + V_{in}\cos\omega t$$

- input cosinusoidal voltage

$$i = \begin{cases} I_q + I\cos\omega t, & -\theta \le \omega t < \theta \\ 0, & \theta \le \omega t < 2\pi - \theta \end{cases}$$

-output current
conduction angle 2θ
indicates its duty cycle

For moment with zero current

$$i = 0 = I_q + I\cos\theta$$

$$\cos\theta = -\frac{I_q}{I}$$

$$i = I\left(\cos\omega t - \cos\theta\right)$$

For moment with maximum current

$$i = I_{max} = I\left(1 - \cos\theta\right)$$

3.4. Class-A,-B,-C operation modes

$I_q = -I\cos\theta$ - quiescent current as function of half-conduction angle θ

- when $\theta > 90°$ $\Rightarrow$ $\cos\theta < 0$ $\Rightarrow$ $I_q > 0$ - Class AB operation mode
- when $\theta = 90°$ $\Rightarrow$ $\cos\theta = 0$ $\Rightarrow$ $I_q = 0$ - Class B operation mode
- when $\theta < 90°$ $\Rightarrow$ $\cos\theta > 0$ $\Rightarrow$ $I_q < 0$ - Class C operation mode

$$i = I_0 + I_1\cos\omega t + I_2\cos 2\omega t + I_3\cos 3\omega t + \ldots$$ - Fourier series

where $$I_0 = \frac{1}{2\pi}\int_{-\theta}^{\theta} I\left(\cos\omega t - \cos\theta\right)d(\omega t) = I\,\gamma_0$$ - DC component

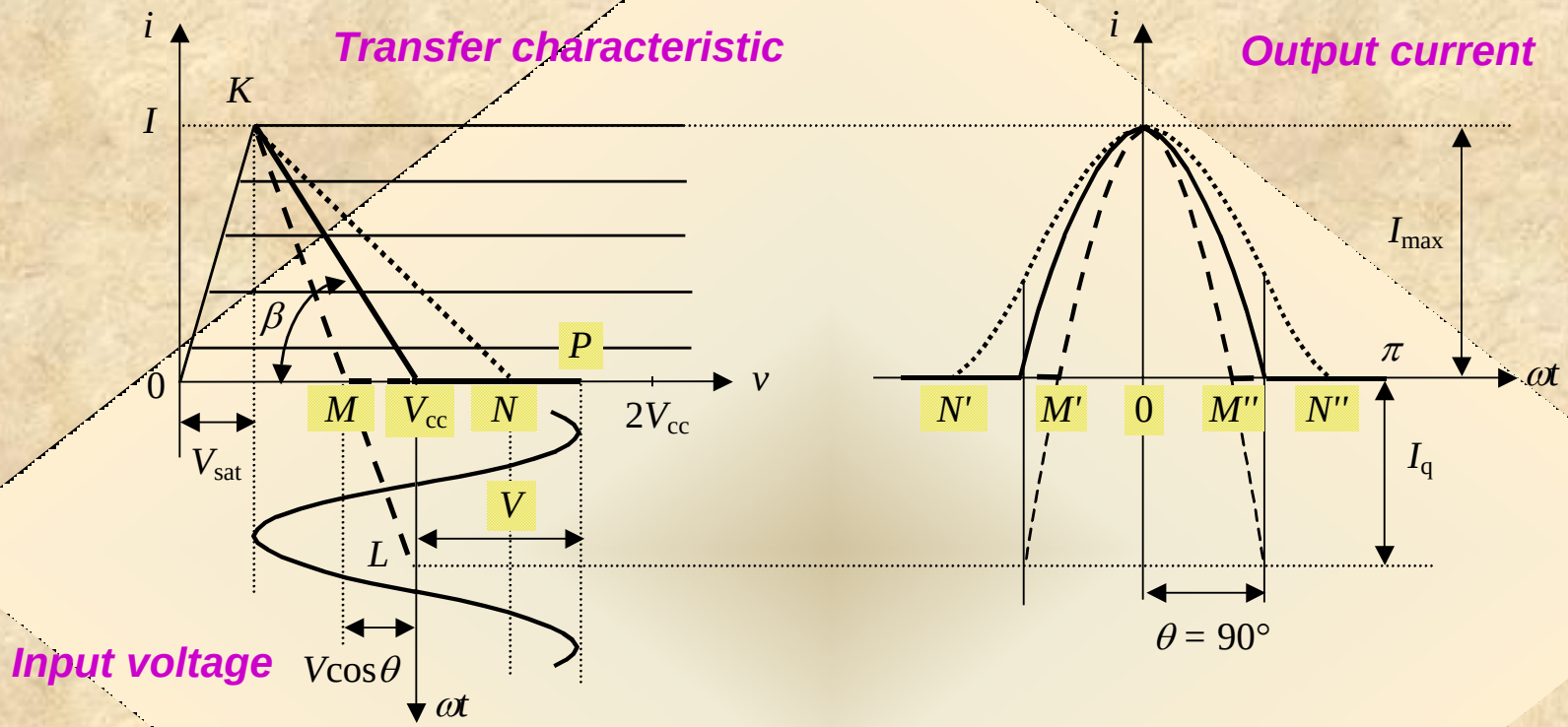
$$I_1 = \frac{1}{\pi}\int_{-\theta}^{\theta} I\left(\cos\omega t - \cos\theta\right)\cos\omega t\, d(\omega t) = I\,\gamma_1$$ - fundamental component

where $$\gamma_0 = \frac{1}{\pi}(\sin\theta - \theta\cos\theta), \quad \gamma_1 = \frac{1}{\pi}(\theta - \sin\theta\cos\theta)$$ - current coefficients

$$\eta = \frac{P_1}{P_0} = \frac{1}{2}\frac{I_1}{I_0}\xi = \frac{1}{2}\frac{\gamma_1}{\gamma_0}\xi$$ - collector efficiency

When $\theta = 90°$ and $\xi = 1$ $\Rightarrow$ $\eta = \frac{\pi}{4} \cong 0.785$ - maximum collector efficiency in Class B

3.4. Class-A,-B,-C operation modes



$$i = \left(I_q + \frac{V_{cc}}{\gamma_1 R} \right) - \frac{v}{\gamma_1 R}$$

- dynamic characteristic of power amplifier or load line function within

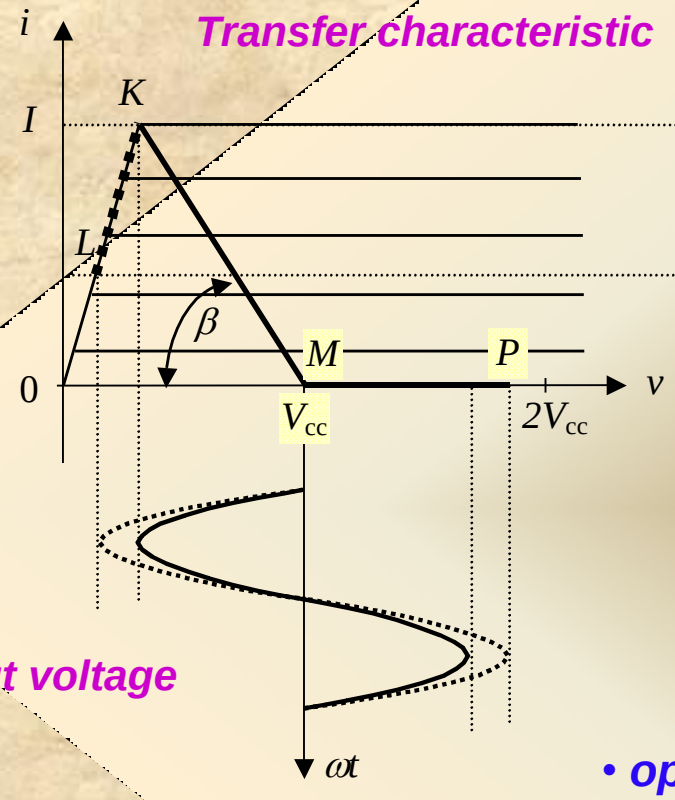
$$-\theta \le \omega t < \theta$$

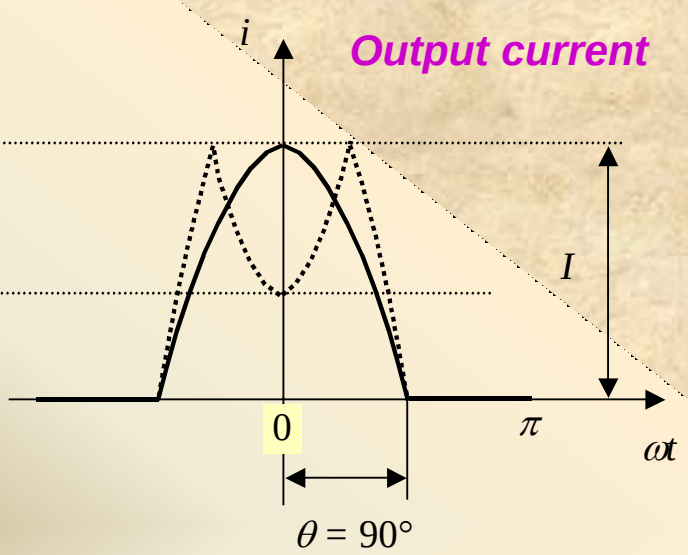
$$\tan\beta = \frac{I}{V(1 - \cos\theta)} = \frac{1}{\gamma_1 R}$$

- slope of load line

3.4. Class-A,-B,-C operation modes

Class B





For increased input voltage amplitude:

- ***operation in saturation, active and pinch-off regions***

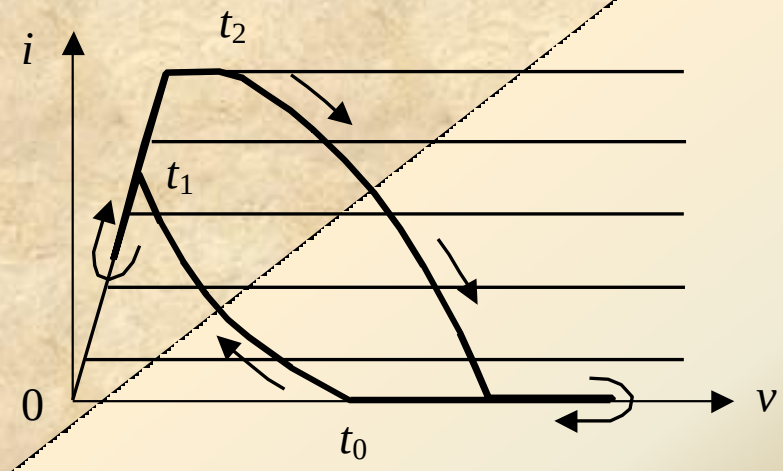
- ***load line represents broken line with three sections:***

  KL- saturation region (depression in collector current waveform)

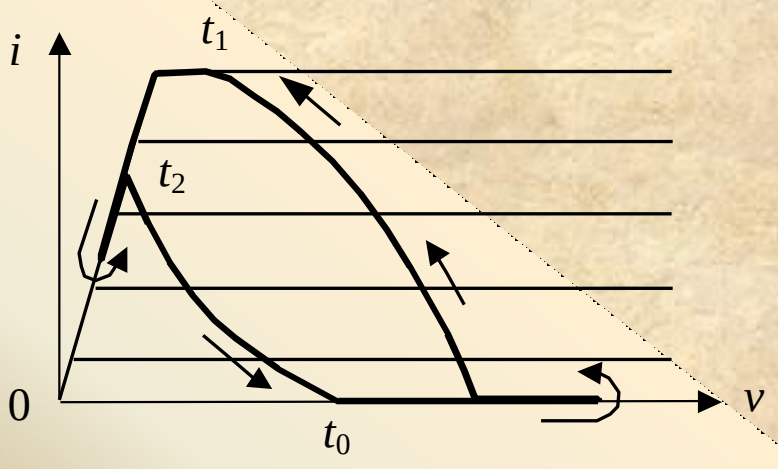
  KM – active region

  MP – pinch-off region

3.4. Class-A,-B,-C operation modes



a).



b).

- ***collector current becomes asymmetrical for complex load impedance***

asymmetrical load line

- ***for inductive load impedance, depression in collector current waveform is shifted to the left (a)***
- ***for capacitive load impedance, depression in collector current waveform is shifted to the right (b)***

Reason: different phase conditions for higher-order harmonics

3.5. Linearity

To evaluate nonlinear properties of power amplifier, consider transfer function of active device in common form of i = f(v) where i - output current, v - input voltage

$$f(v) = f(V_0) + \sum_{n=1}^{\infty} \frac{1}{n!} \frac{\partial^{(n)} f(v)}{\partial v^n}\bigg|_{v=V_o} (v - V_0)^n$$

where V_0 - DC bias voltage

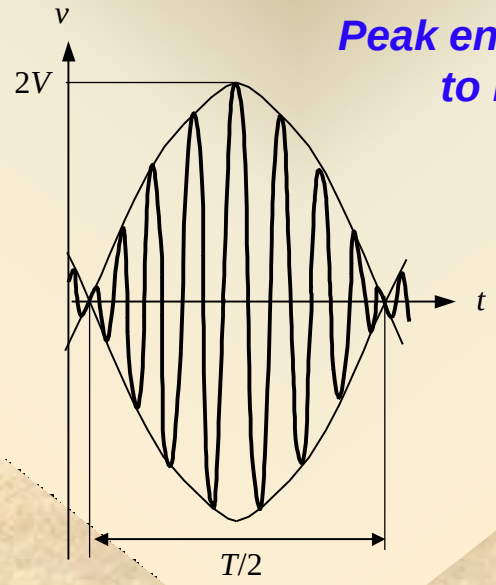
Usual method to determine nonlinear properties is to to apply two-tone excitation test signal

For two signals with equal amplitudes $V_1 = V_2 = V$:

$$v = V_1 \cos \omega_1 t + V_2 \cos \omega_2 t$$
$$= 2V \cos \omega t \cos \Omega t$$

where

$$\omega = (\omega_1 + \omega_2)/2$$
$$\Omega = (\omega_1 - \omega_2)/2$$



Peak envelope power PEP corresponds to maximum amplitude of 2V:

$$P_{PEP} = (2V)^2 / 2R$$

Total power due to each tone:

$$P_{total} = P_{\omega 1} + P_{\omega 2} = V^2 / R$$

$$P_{PEP} = 2P_{out} = 4P$$

where $P = P_{\omega 1} = P_{\omega 2}$

3.5. Linearity

For two-tone excitation test signal $v = V_0 + V_1\cos\omega_1 t + V_2\cos\omega_2 t$

Taylor's expansion of output current for first three derivatives results in

$$i = f(v) = f(V_0) + \frac{1}{4}\left.\frac{\partial^2 f(v)}{\partial v^2}\right|_{v=V_o}\left(V_1^2 + V_2^2\right)$$

$$+\left[f'(V_0) + \frac{1}{4}\left.\frac{\partial^3 f(v)}{\partial v^3}\right|_{v=V_o}\left(\frac{1}{2}V_1^2 + V_2^2\right)\right]V_1\cos\omega_1 t + \left[f'(V_0) + \frac{1}{4}\left.\frac{\partial^3 f(v)}{\partial v^3}\right|_{v=V_o}\left(V_1^2 + \frac{1}{2}V_2^2\right)\right]V_2\cos\omega_2 t$$

$$+\frac{1}{4}\left.\frac{\partial^2 f(v)}{\partial v^2}\right|_{v=V_o}\left(V_1^2\cos 2\omega_1 t + V_2^2\cos 2\omega_2 t\right) + \frac{1}{24}\left.\frac{\partial^3 f(v)}{\partial v^3}\right|_{v=V_o}\left(V_1^3\cos 3\omega_1 t + V_2^3\cos 3\omega_2 t\right)$$

$$+\frac{1}{2}\left.\frac{\partial^2 f(v)}{\partial v^2}\right|_{v=V_o}V_1 V_2\cos\left(\omega_1 \pm \omega_2\right)t$$

$$+\frac{1}{8}\left.\frac{\partial^3 f(v)}{\partial v^3}\right|_{v=V_o}\left[V_1^2 V_2\cos\left(2\omega_1 \pm \omega_2\right)t + V_1 V_2^2\cos\left(\omega_1 \pm 2\omega_2\right)t\right]\ldots$$

3.5. Linearity

Main conclusions:

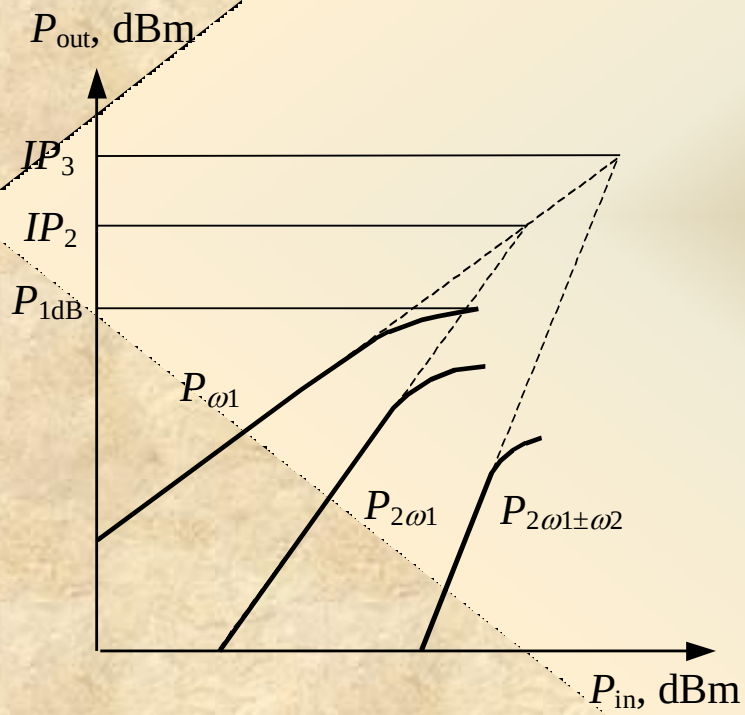
- *variation of DC bias point is directly proportional to second derivative (in common case - even derivatives) of transfer function*
- *device transfer function will be linear only if third derivative (in common case - odd derivatives) is equal to zero*
- *even harmonic components are result of even derivatives of transfer function; odd harmonic components are result of odd derivatives of transfer function*
- *first-order mixing products (total and differential) depend on even derivatives of transfer function*
- *mixing products of third and higher order are mainly determined by odd derivatives of transfer function*

Distortions which are determined by second derivatives of device transfer function are called second-order intermodulation distortions; distortion which are determined by third-order derivatives are called third-order intermodulation distortions

3.5. Linearity

Output current amplitude of fundamental, second and third harmonic or intermodulation components depends on first, second and third degree of input voltage, respectively

Consequently, output powers of linear, second- or third-order component show straight-line behavior and vary by 1 dB, 2 dB and 3 dB, respectively, with 1-dB variation of input power



These straight lines intersect at some points which are called intercept points IP_n

$$P_{IM_n} = nP_{\omega_1} - (n-1)IP_n \text{ (dBm)}$$

Second harmonic component

$$P_{2\omega_1} = 2P_{\omega_1} - IP_2 \text{ (dBm)}$$

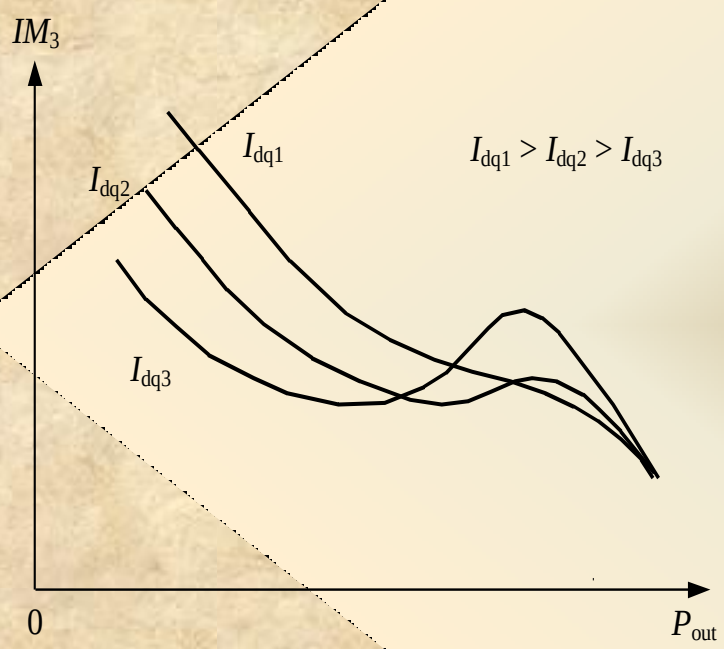
Third-order intermodulation component

$$P_{2\omega_1-\omega_2} = 3P_{\omega_1} - 2IP_3 \text{ (dBm)}$$

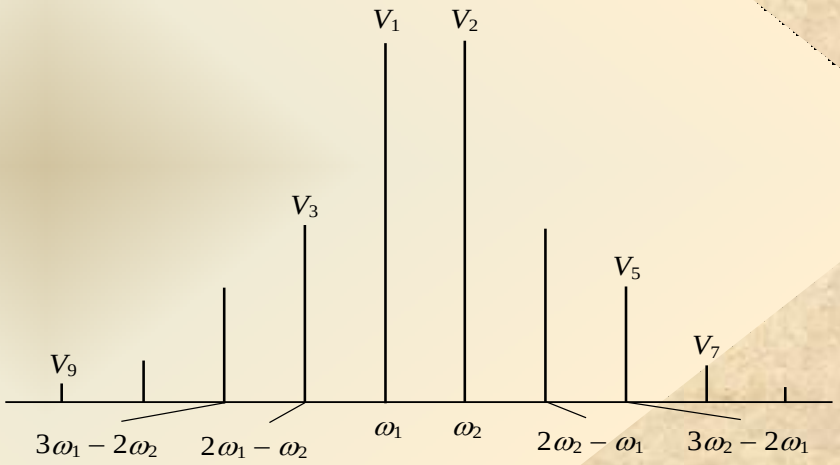
$$P_{1dB} = IP_3 - 9 \text{ (dBm)}$$ ***- 1-dB gain compression point***

3.5. Linearity

For MOSFET device, there is optimum bias point with drain quiescent current I_{dq} in limits of 0.1…0.15 I_{dss} when IM_3 can be minimized providing high-power and high-efficiency operation because of quadratic transfer function in this region



Output spectrum containing n-order intermodulation components



$$IM_3 = 10\log_{10}\left(P_{2\omega_1-\omega_2} / P\right) = P_{2\omega_1-\omega_2} - P \ (\text{dBc})$$

- third-order intermodulation product

$$IM_5 = 10\log_{10}\left(P_{3\omega_1-2\omega_2} / P\right) = P_{3\omega_1-2\omega_2} - P \ (\text{dBc})$$

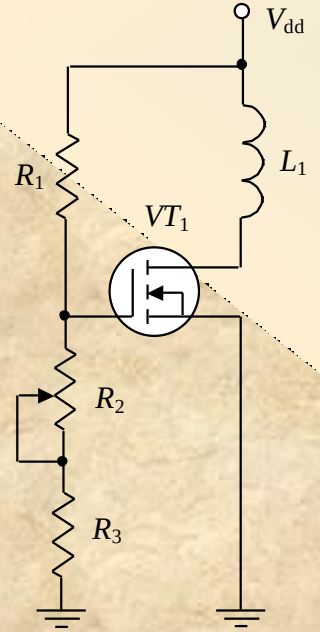
- fifth-order intermodulation product

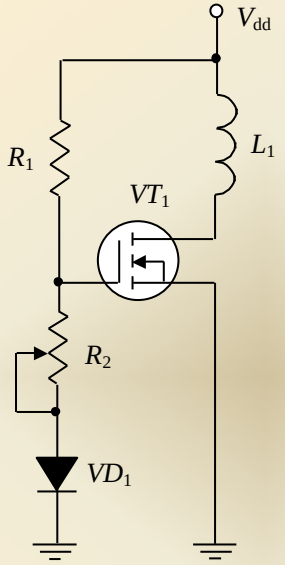
where $P = P_{\omega_1} = P_{\omega_2}$

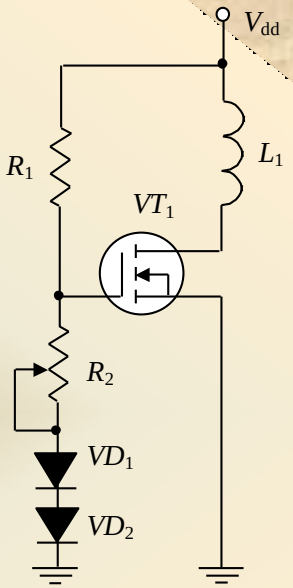
3.6. DC biasing

DC biasing of active device provides required operation condition which should be stable over input power, temperature or technology process variations

For MOSFETs as voltage controlled devices, at normal conditions it is enough to use resistive divider to set gate bias voltage







When device threshold voltage is too high, it is best to connect several silicon diodes in series

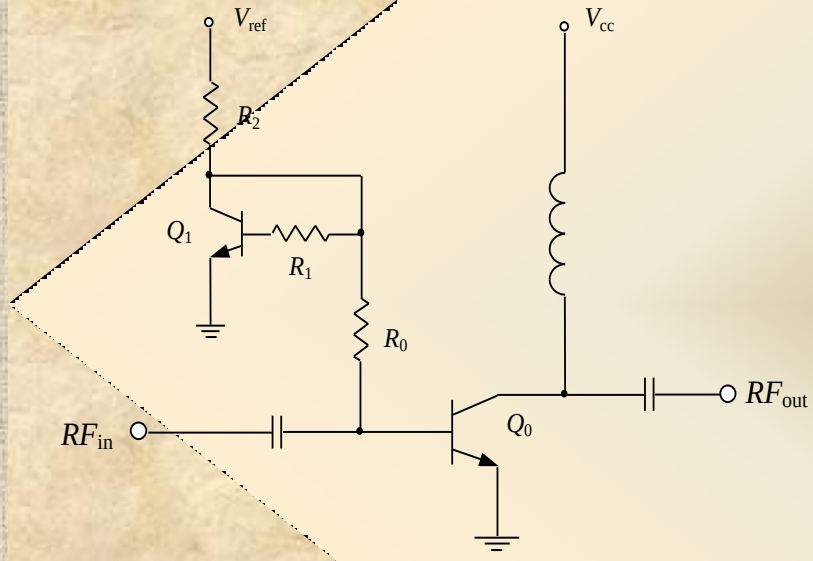
However, in wide temperature range when device threshold voltage varies with temperature (2 mV/℃), to reduce quiescent current variation, it is possible to use silicon diode in series to variable resistor

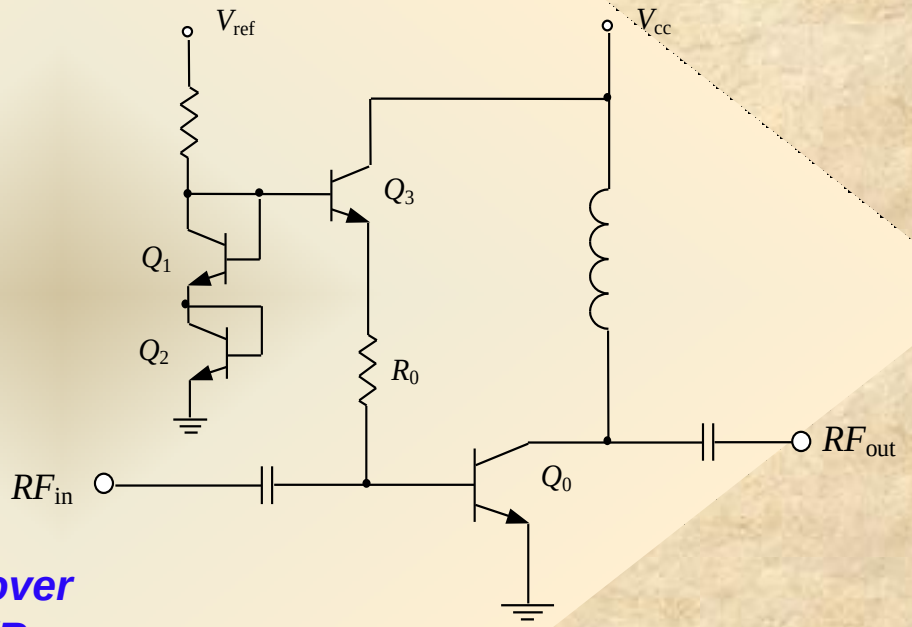
Such simple bias circuit configurations for MOSFETs become possible in view of extremely small gate DC current equal to its leakage current only

3.6. DC biasing

Current mirror bias circuits

For bipolar transistor as current-controlled device, to stabilize quiescent current it is best to use current-mirror type of bias circuits where reference diode is formed using same diode-connected transistor with substantially smaller area





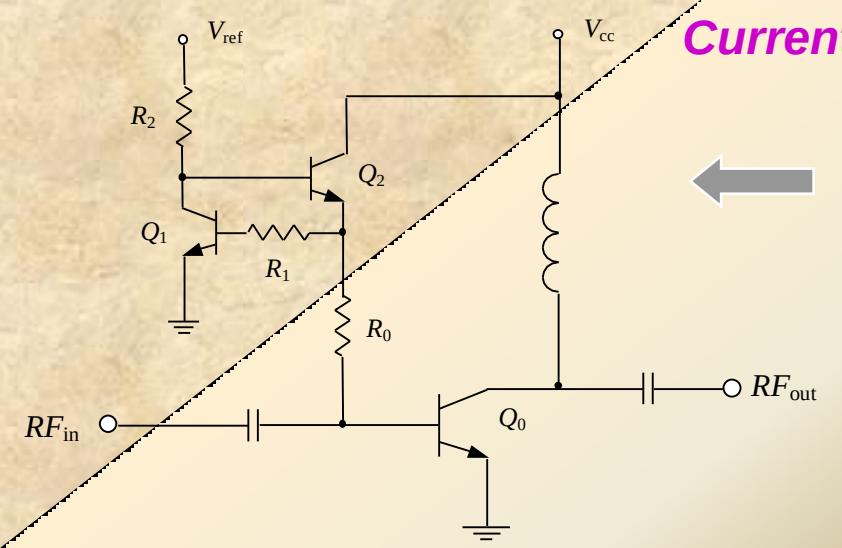
To minimize quiescent current variations over temperature, ratio of ballast resistors R_1/R_0 must be equal to device area ratio Q_0/Q_1

However,to fix current flowing from reference source through resistor R_2, its value should be much higher than base current of RF device Q_0

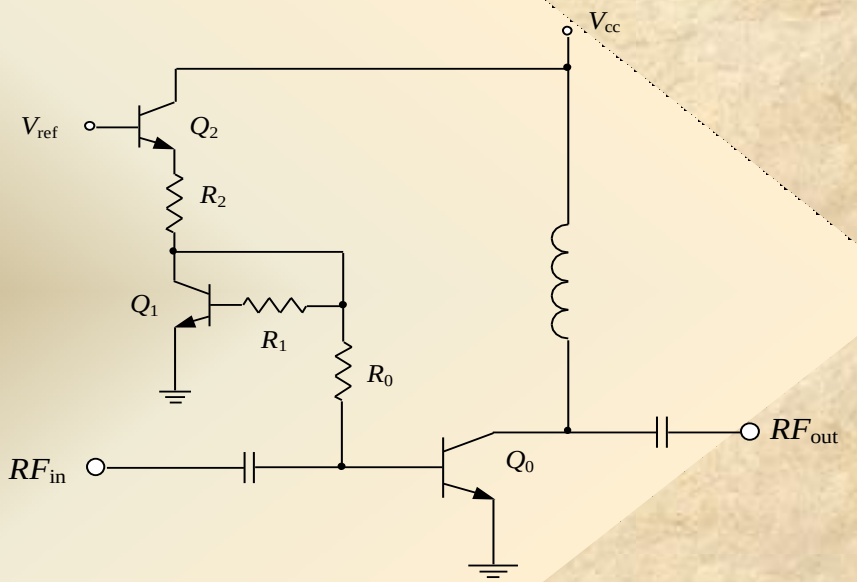
To reduce current from reference source and to increase current driving capability for high power RF device, driving transistor Q_3 is used to feed DC base current for RF device Q_0

3.6. DC biasing

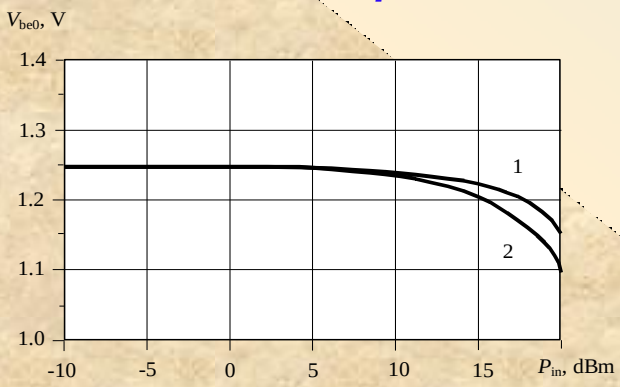
Current mirror bias circuits



Popular configuration of temperature compensated bias circuit contains one reference transistor and one driving device



It is very important to provide ratio of ballast resistors R_1/R_0 equal to ratio of device areas Q_0/Q_1 which minimizes variations over temperature as well as stabilizes DC bias point over input power



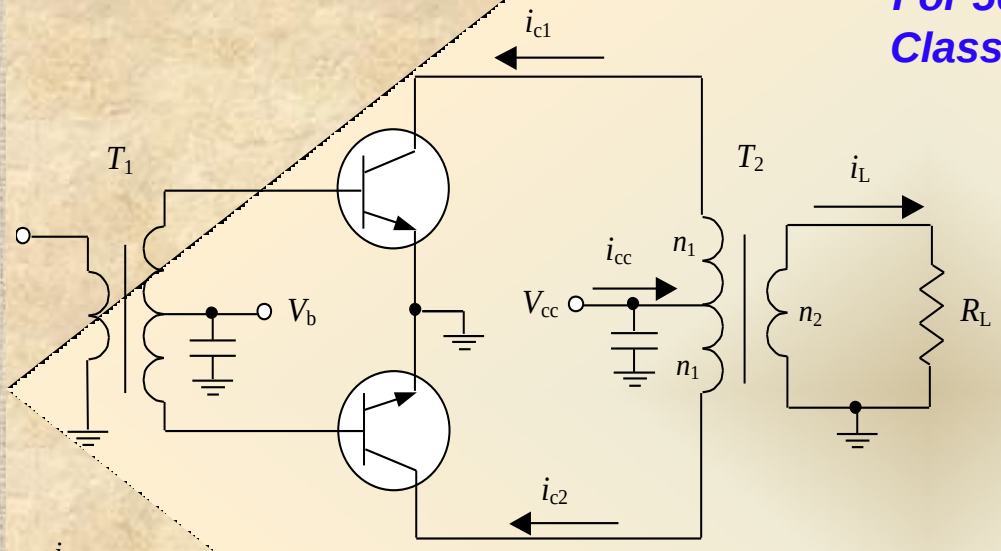
1 - required value of ballast resistor R_1

2 - $R_1 = 0$

To minimize current from reference voltage source, emitter follower configuration can be used where this current is equal to extremely small base current of emitter follower device Q_2

3.7. Push-pull amplifiers

Push-pull operation helps to increase values of input and output impedances and to additionally suppress even harmonics



For 50% duty cycle of each device (ideal Class B) with driving sinusoidal voltage:

first transistor collector current

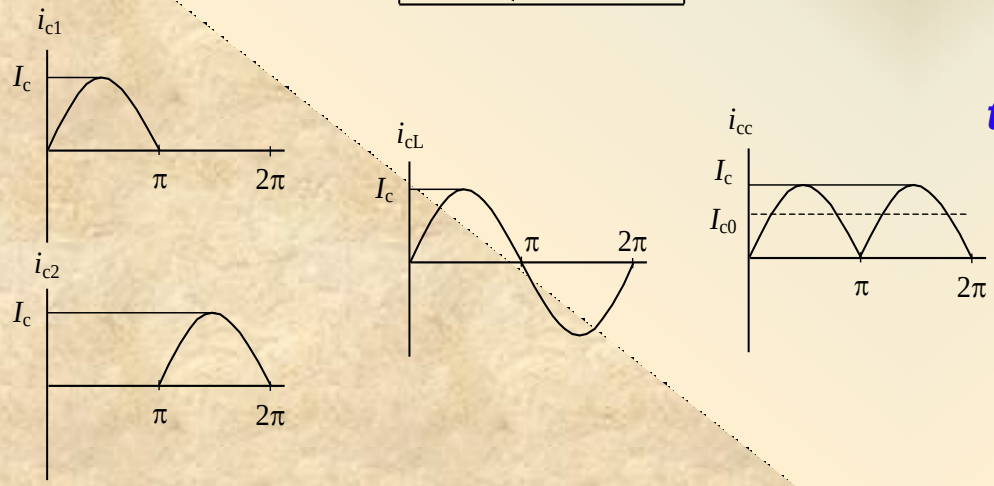
$$i_{c1} = \begin{cases} +I_c \sin\theta, & 0 \le \theta < \pi \\ 0, & \pi \le \theta < 2\pi \end{cases}$$

second transistor collector current

$$i_{c2} = \begin{cases} 0, & 0 \le \theta < \pi \\ -I_c \sin\theta, & \pi \le \theta < 2\pi \end{cases}$$

Being transformed through output transformer T_2, total collector current:

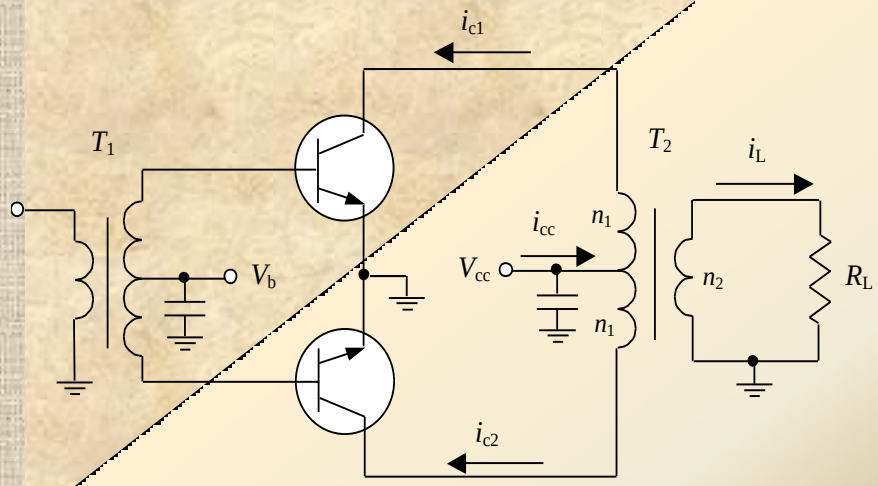
$$i_L(\theta) = i_{c1}(\theta) - i_{c2}(\theta) = I_c \sin(\theta)$$



Current flowing in center tap of primary winding of transformer T_2:

$$i_{cc}(\theta) = i_{c1}(\theta) + i_{c2}(\theta) = I_c \left| \sin(\theta) \right|$$

3.7. Push-pull amplifiers



Ideally, even-order harmonics are canceled as they are in-phase and combined in center tap of primary winding of output transformer

To eliminate losses, it is necessary to connect bypass capacitance to this center point

As for 50% duty cycle, third- and higher-order odd harmonics do not exist, ideally sinusoidal signal will appear in load

$$v_L(\theta) = I_c R_L \sin(\theta) = V_L \sin(\theta)$$

Total DC collector current

$$I_{co} = \frac{1}{2\pi}\int_0^{2\pi} i_{cc}(\theta)\,d\theta = \frac{2}{\pi} I_c$$

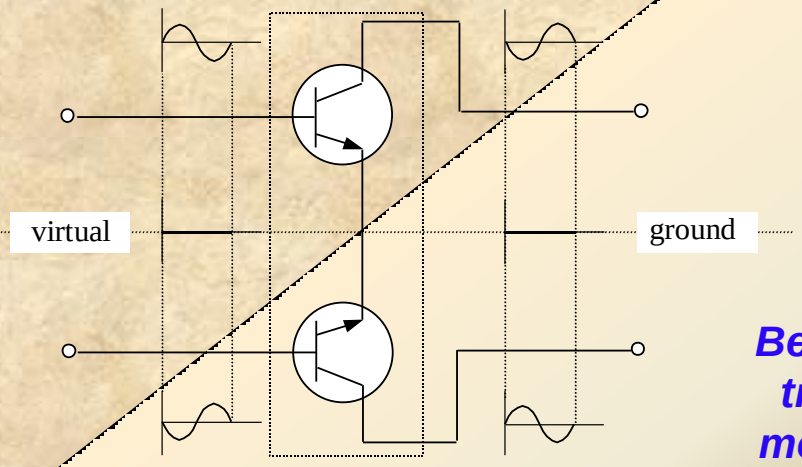
For zero saturation resistance when collector voltage amplitude $V_c = V_{cc}$ and equal turns of winding when $V_L = V_c$, DC and fundamental output powers

$$P_0 = \frac{2}{\pi} I_c V_{cc} \qquad P_{out} = \frac{1}{2} I_c V_{cc}$$

Maximum theoretical collector efficiency that can be achieved in Class B operation

$$\eta = \frac{P_{out}}{P_0} = \frac{\pi}{4} \cong 78.5\%$$

3.7. Push-pull amplifiers



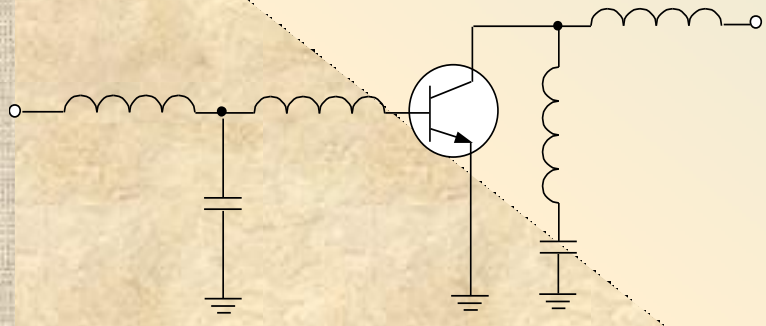
In balanced circuit, identical sides carry 180° out-of phase signals of equal amplitude

If perfect balance is maintained, there are midpoints where signal amplitudes are zero

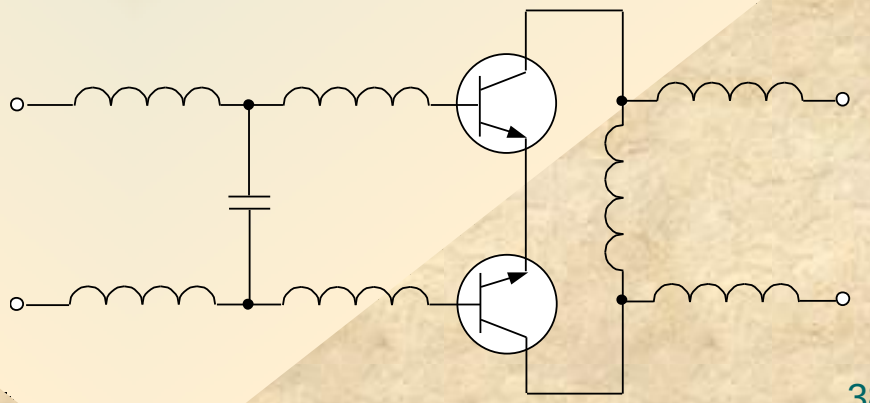
Such a condition is called virtual grounding

Being inside device package with two balanced transistors, virtual ground reduces common-mode inductance and simplify matching circuit

Matching conditions for single-ended transistor

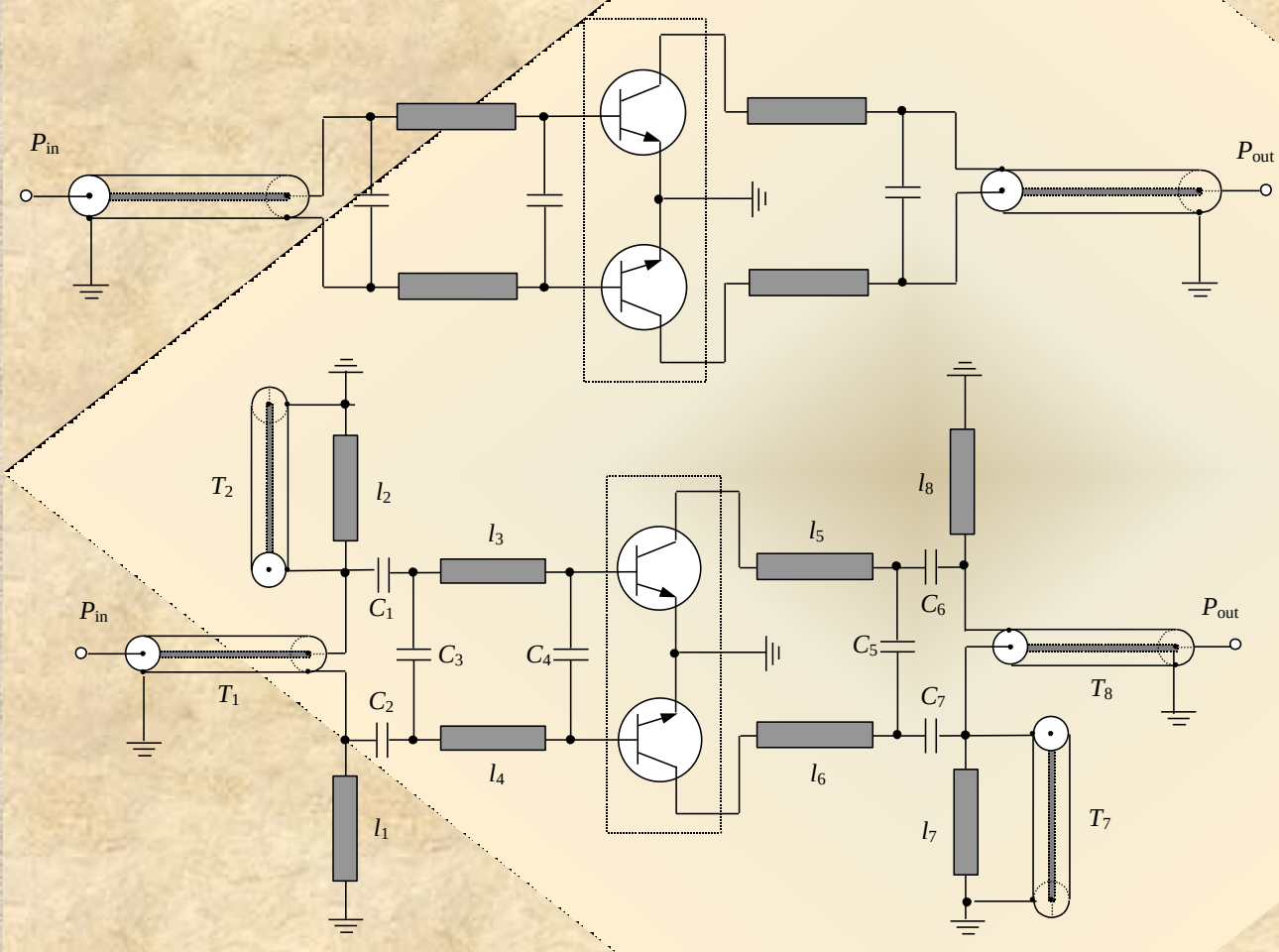


Simplification for balanced transistors where matching parallel capacitances are combined and DC blocking capacitances are not required



3.7. Push-pull amplifiers

For push-pull operation, unbalance-to-balance transformation is required

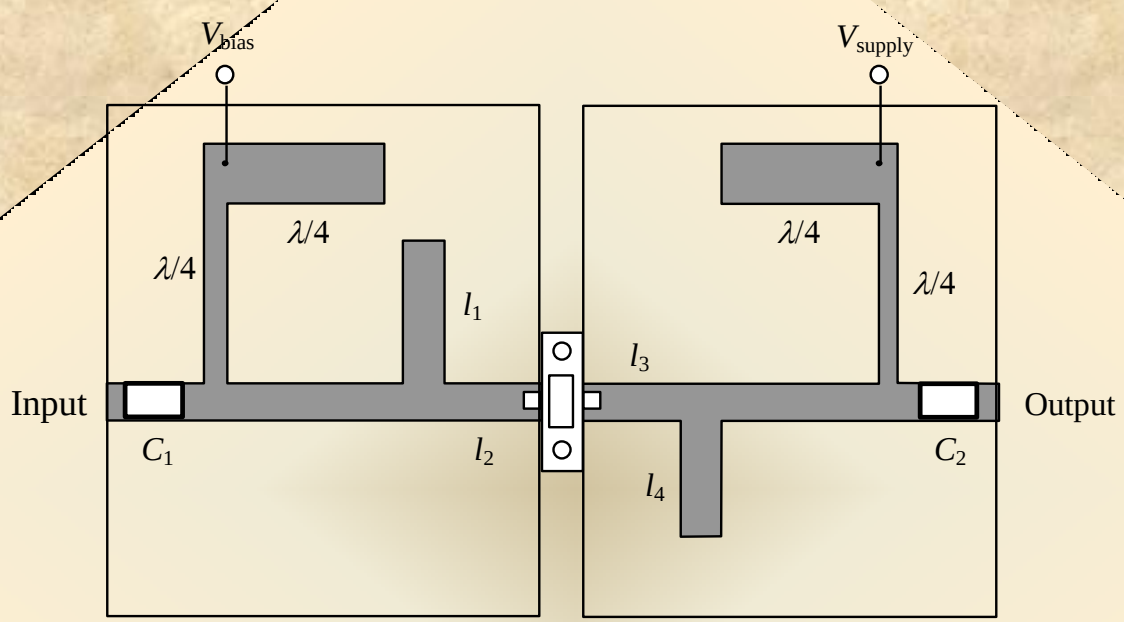


- ***most suitable approach is to use 1:1 coaxial transformer***
- ***for 50-ohm source and load, its characteristic impedance = 50 Ohm and each balanced part sees 25 Ohm***
- ***to minimize transformer size and provide broadband operation with minimum return loss, coaxial transformers are mounted and soldered along shortened microstrip lines and additional shortened stubs are added for symmetry***

- ***as shortened stubs produce inductive impedances, series capacitors C_1 and C_2 are used forming high-pass matching sections***

3.8. Practical aspect of RF and microwave power amplifiers

Typical microwave power amplifier topology

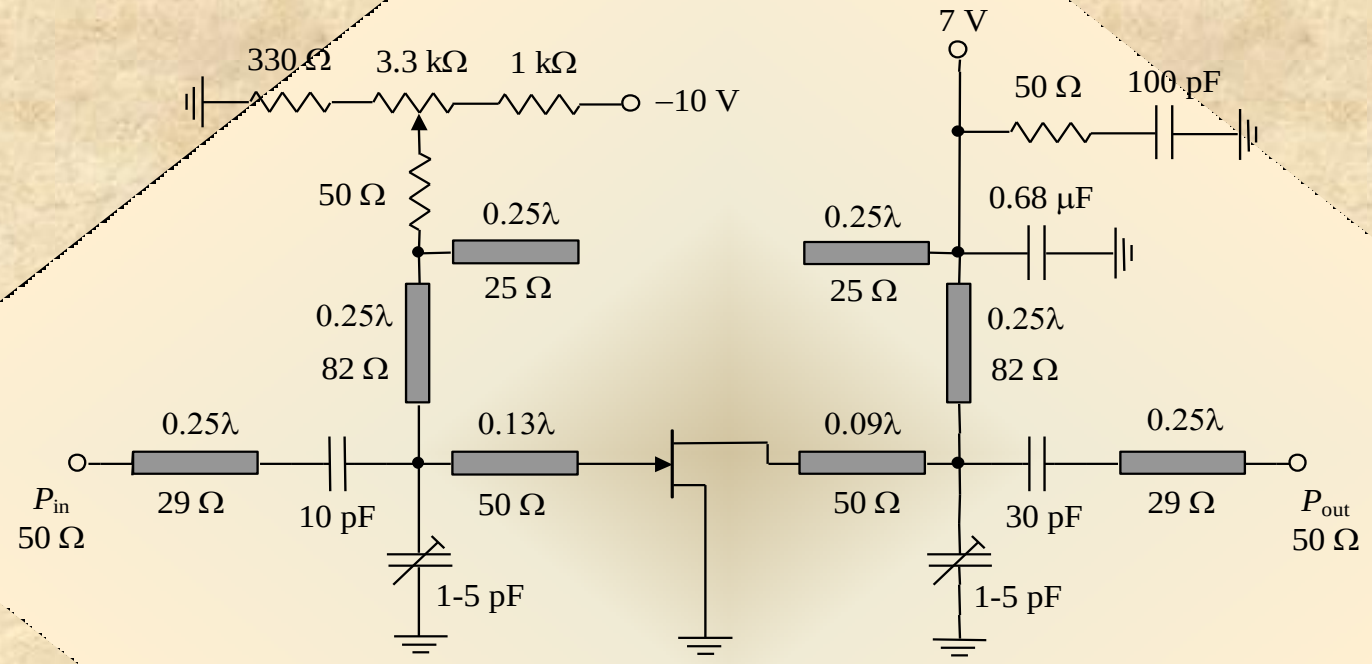


- ***matching circuits in form of L-transformers: parallel microstrip open stubs represent capacitive reactances, series microstrip lines represent inductive reactances***

- ***bias circuits contain quarterwave loaded and opened microstrip lines for RF signal isolation***

3.8. Practical aspect of RF and microwave power amplifiers

Microwave 2.5-2.7 GHz 5 W GaAs MESFET power amplifier topology

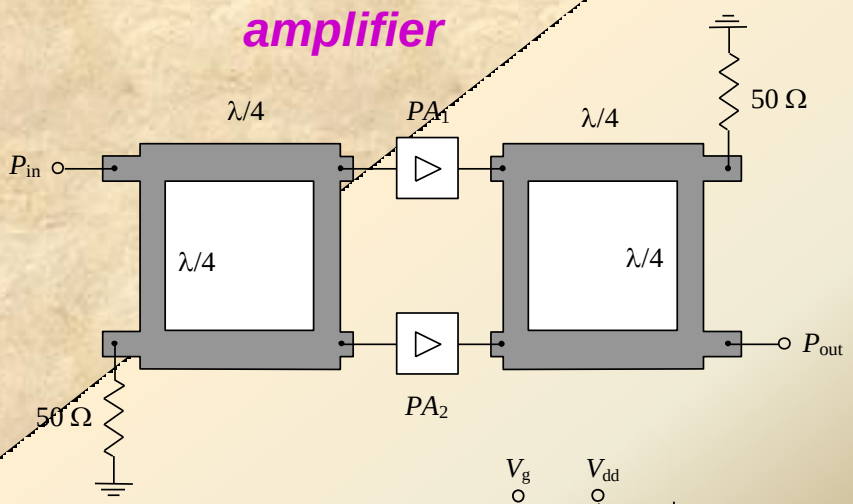


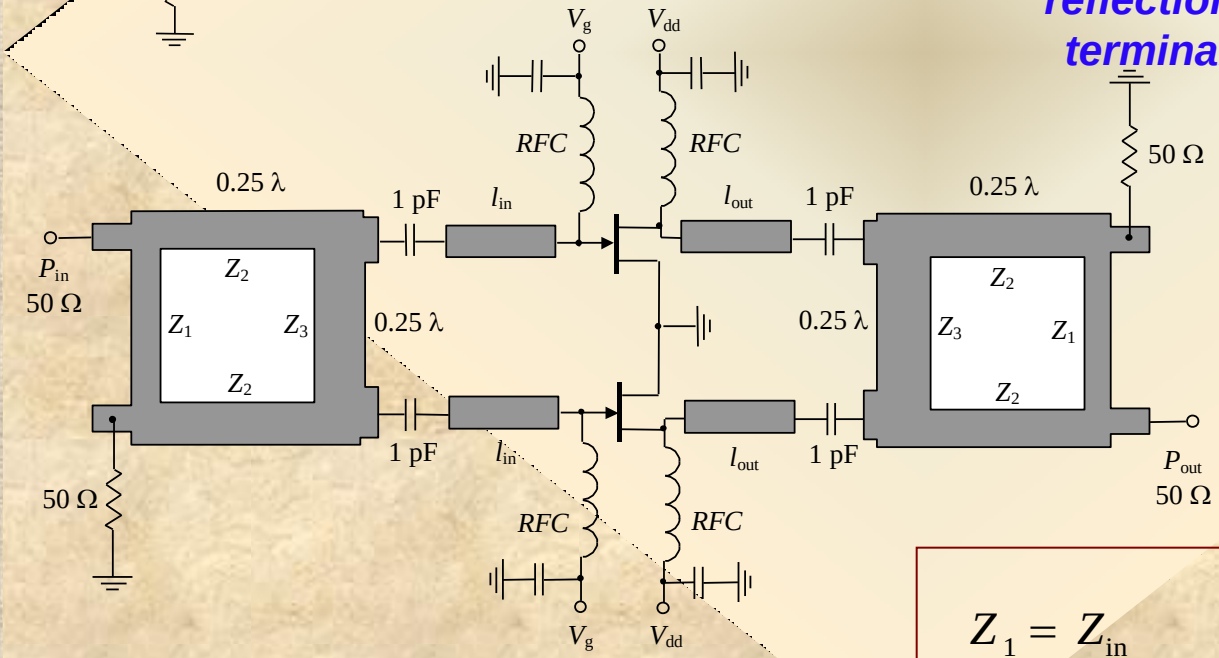
- *matching circuits are combinations of L-transformers (parallel capacitors and series microstrip lines) and quarterwave lines with different characteristic impedances*

- *drain bias circuit contains additional RC-circuit to prevent high-frequency oscillations and large capacitance to prevent low-frequency oscillations*

3.8. Practical aspect of RF and microwave power amplifiers

Microwave balanced power amplifier



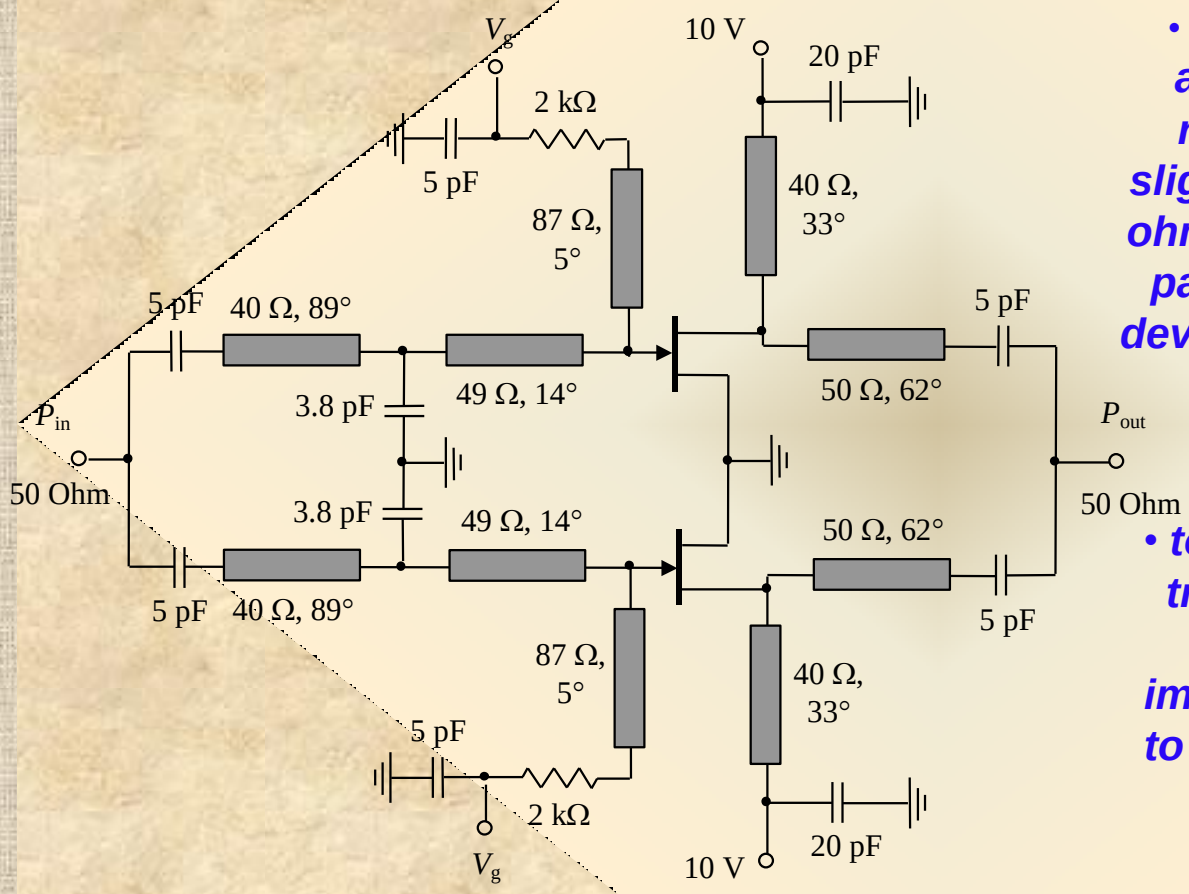


- *to combine output powers from two or more transistors at microwaves, 90-degree branch-line hybrids are widely used where active devices are isolated from each other*
- *at equal reflection coefficients from loads connected to output terminals, reflection wave is absent at input terminal and flowing to 50-ohm ballast resistor*
- *branch-line hybrid also can work as impedance transformer with characteristic impedances of its microstrip branches as*

$$Z_1 = Z_{in} \qquad Z_3 = Z_{out} \qquad Z_2 = \sqrt{\frac{Z_{in} Z_{out}}{2}}$$

3.8. Practical aspect of RF and microwave power amplifiers

Microwave 5.5 GHz 2.5 W GaAs MESFET power amplifier topology



- *for monolithic microwave applications, when output resistance of transistor is slightly less or higher than 50-ohm, it is convenient to realize parallel connection of active devices (easy to provide circuit symmetry for packaged devices)*
- *to combine power from two transistors, it is necessary simply to transform impedance from each device to 100 Ohm and then parallel connection results in required 50-ohm load*

- *input matching circuits represent quarterwave microstrip line transformer and L-transformer with series microstrip line and parallel capacitance each*