Microwave Transistors: Theory and Design

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Abstract—Microwave transistors are useful as small-signal amplifiers to 6 GHz and power amplifiers to 4 GHz. Nearly all microwave transistors are of the silicon planar type. Power transistors use three types of geometries—interdigitated, overlay, and mesh—while small-signal transistors use interdigitated only. The general theory of the frequency response of transistors is reviewed, including active and inactive elements. A condensed description of the design and processing steps for a silicon microwave transistor is given. A final section deals with the types of high-frequency measurements used in the design and analysis of transistors.

I. Introduction

MICROWAVE transistors have come to be regarded as a pinnacle in the transistor art. Not only are they difficult to build, but most of the more desirable parameters have been optimized. Because of the very fine geometry and the shallow diffusions which are used, yields have remained relatively modest compared to low-frequency types. This is in spite of the fact that a 1.5-in-diam silicon slice has a potential of almost 8000 transistors on 0.015-in centers.

The maximum frequency of oscillation now exceeds 15 GHz for the typical small-signal transistor. Noise figures less than 1 dB are now attained at 500 MHz, and less than 6 dB at 6 GHz. Power output is also impressive—a peak of 100 W at 1 GHz and 5 W CW at 4 GHz. Fig. 1 gives a plot of noise figure and power output versus frequency as of November 1970.

If oscillation or useful gain above 1 GHz is taken as the criterion for microwave operation, the germanium mesas and microalloy transistors of the 1958–1959 era were the first microwave transistors. The advantages of germanium over silicon as a semiconductor material, however, remained largely theoretical, and by 1963 silicon microwave transistors were beginning to become competitive. From the point of view of the user, the relative ruggedness of the silicon transistor was decisive and the phaseout of germanium was begun.

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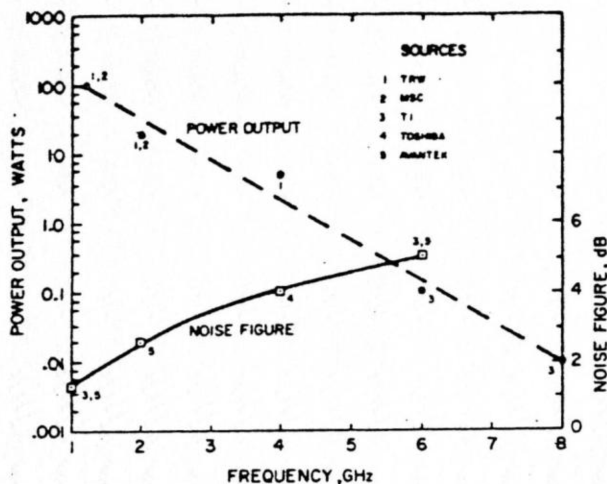

Fig. 1. Noise figure and power output of microwave transistors, November 1970.

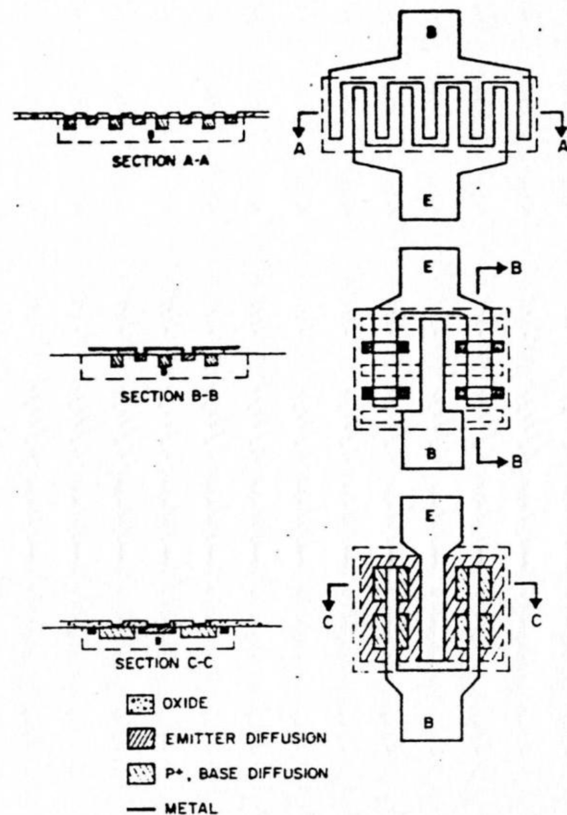

Fig. 2. Three general types of microwave transistor geometry.

Today a few germanium, *L*-band, planar transistors are still in use, but their numbers are decreasing rapidly. One very important reason for the demise of the high-frequency germanium transistor is that germanium does not have a natural passive oxide. For this reason, germanium planar transistors use silicon oxide as the passivating agent.

This paper will attempt to give a broad picture of the theory, construction, and testing of microwave transistors. The details of some areas which are largely descriptive (such as power transistor design) will be discussed only from the basic theoretical point of view. Where processes or theory are common to low-frequency transistors, only a brief mention will be given.

The Introduction will be completed with a brief description of the general structure of microwave transistors.

All microwave transistors are now planar in form and almost all are silicon n-p-n. The geometry falls into three general types (Fig. 2): 1) interdigitated, for small signal and power; 2) overlay, for power only; and 3) mesh (also called "matrix" and "emitter grid"), for power only. Several analyses [1] have been made comparing these three structures on an idealized basis; the conclusions reached tend to become less clear when practical devices are considered. It can be shown, however, that where one structure displays a definite superiority in some respect, it is achieved at the expense of a degradation of one or more other parameters. This is particularly true with respect to capacitance, where reduced C_{TE} is obtained at the expense of high MOS capacitance, etc.

It appears now that the overlay and mesh structures are beginning to dominate the VHF–UHF power device market while the interdigitated transistor is still the best structure for *S*- and *C*-band small-signal applications.

Most power transistors now include some form of integral emitter resistors to aid in equalizing the current distribution over the larger area which a power device must cover. The overlay transistor uses an integral diffused resistor as part of the emitter itself, while the interdigitated generally use thin-film resistors as a part of the contact system. Mesh devices [1], [2] have been constructed using both techniques. Some earlier devices used separate diffused resistors mounted on the package.

The use of silicon nitride as an additional passivating agent is fast becoming universal. It has a particular value in microwave transistors where the junctions are extremely shallow and thus highly susceptible to contamination.

Silicon nitride is a superior passivating agent (compared to silicon dioxide), although it cannot be placed directly over a bipolar transistor junction. A thin layer of SiO_2 is usually placed between it and the silicon. Since it is not etched at the same rate as SiO_2 by hydrofluoric acid etches, it has some advantages as a secondary mask. Junctions passivated with it have a lower failure rate and can operate at a higher temperature.

The current carrying capability of a transistor is proportional to the emitter periphery, base resistance is inversely proportional to the emitter width, and f_T (at lower currents) is inversely proportional to the emitter area. Thus a good microwave transistor has a very narrow emitter (e.g., ≈ 1.0 μm, for state of the art). To keep the length to a practical size, the device is broken up into emitter "sites." These sites may be grouped together (overlay) or simply connected in parallel (interdigitated). Some of the more sophisticated mesh and interdigitated types for high power also group the emitters into secondary sites.

II. Transistor Theory

A. Performance

1) Gain: In this section the theory of transistor action, insofar as the high-frequency characteristics are concerned, will be reviewed. Appropriate equations will be used where required, but proofs and developments will be shortened or presented by reference only.

A good microwave transistor must, first of all, be a good dc transistor. Most of the requirements for good dc operation can be satisfied independently of the high-frequency requirenents and where exceptions occur, such as the effect of a drift field on the dc current gain, these will be mentioned.

Before discussing gain, it should be pointed out that there are several definitions of gain which are useful for transistor charac-

terization. Maximum available gain (MAG), G_{max}, is obtained when both input and output are simultaneously conjugately matched. G_{max} exists only when the device is unconditionally stable. Unilateral gain, or U [3], is obtained when a device is unilateralized with a lossless network and matched at both ports. U is the same common base, common collector or common emitter. In the microwave region, U is 1-3 dB higher than G_{max}, common emitter, for a typical small-signal transistor. Both G_{max} and U are often defined in terms of f_{max}, and both should drop to unity at about that frequency. Since common-emitter microwave transistors may have power gain with no impedance transformation, they can have useful gain when inserted directly into a 50-Ω system. This gain is identical to $|S_{21}|^2$.

The general form for the gain as a function of frequency is

$$G(f) \approx \frac{G_0}{\left[1 + G_0^2\left(\frac{f}{f_{max}}\right)^4\right]^{1/2}}. \quad (1)$$

When $G_0^2(f/f_{max})^4 >> 1$, $G \approx (f_{max}/f)^2$ and gain falls at 6 dB per octave. The gain function is actually discontinuous, and there are regions of potential instability where gain is undefined. Fig. 3 shows these regions for the common-base and common-emitter configurations.

Equation (1) shows that f_{max} is a suitable frequency for defining microwave gain and it is useful, then, to examine f_{max} and the parameters that govern it.

If feedback is considered negligible (or neutralized by a lossless network), a common-emitter transistor can be considered as having the following simplified parameters:

$$\mathrm{Re}(Y_{in}) \approx \frac{1}{r_b'}$$

$$\mathrm{Re}(Y_{out}) \approx \omega_T C_C$$

current gain

$$|h_{fe}| = \frac{\omega_T}{\omega}.$$

The equivalent circuit of Fig. 4 depicts how the parameters fit into a simplified high-frequency equivalent circuit.

The gain of this two-port at ω is

$$G \approx \frac{\omega_T}{4\omega^2 r_b' C_C}. \quad (2)$$

At f_{max} the gain G will have dropped to one, and

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi r_b' C_C}}. \quad (3)$$

A more practical expression is

$$f_{max\,GHz} \approx 6.3\sqrt{\frac{f_T \text{ in GHz}}{(r_b' C_C) \text{ in ps}}}. \quad (3a)$$

This is an approximate expression based on a simplified model; a later section on modeling will present a more accurate model. Note the three critical parameters, f_T, r_b', and C_C.

2) *Noise Figure:* In addition to having gain, small-signal transistors are usually required to have a low enough noise figure to meet certain systems requirements. The noise figure is simply a measure of the degradation in the signal-to-noise ratio that a signal undergoes when passing through a signal processing element, such as a transistor amplifier.

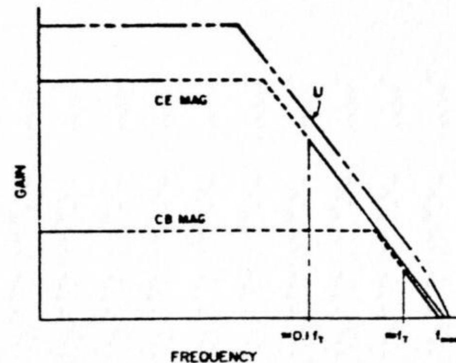

Fig. 3. Maximum available gain and U versus frequency. Broken line represents regions of potential instability.

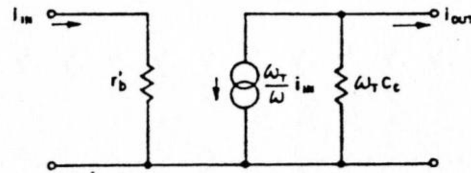

Fig. 4. Simplified equivalent circuit of a transistor for gain calculations. $\mathrm{Re}(Y_{in}) \cong 1/r_b'$ and $\mathrm{Re}(Y_{out}) \cong \omega_T C_C$.

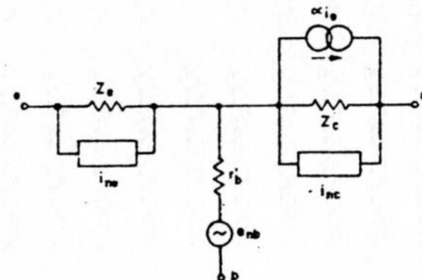

Fig. 5. Common-base transistor noise equivalent circuit.

$$\text{Noise figure } F = \frac{\text{signal-to-noise ratio at input}}{\text{signal-to-noise ratio at output}}.$$

It will be convenient here, as in the previous section on gain, to present a simplified model in order to develop an expression for noise figure. A number of papers have been written on the noise figure of transistors but Nielsen's [4] was the first to present it in terms of generally known transistor parameters. Cooke [5] manipulated Nielsen's equations to give a version which uses more accessible parameters. Fukui's paper [6] presents an exhaustive investigation into transistor noise figure including parasitics.

Fig. 5 is a simplified noise model of a common-base amplifier. The common-emitter amplifier can be treated in the same manner, but the result is the same, and the calculations are more tedious. Fig. 5 shows that in the microwave region the transistor has three principal sources of noise.

a) Shot noise in the emitter:

$$\overline{i_{ne}^2} = 2qI_E\Delta f = 2kTg_e\Delta f. \quad (4)$$

b) Shot noise in the collector:

$$\overline{i_{sc}^2} = 2qI_c\Delta f. \tag{5}$$

c) Thermal noise in the base resistance:

$$\overline{e_{nb}^2} = 4kTr_b'\Delta f. \tag{6}$$

Terms a) and b) are correlated by alpha.

Using the Cooke method [5], the noise figure can be shown to be as follows:

$$F = 1 + \frac{r_b'}{R_g} + \frac{r_e}{2R_g} + \frac{(R_g + r_b' + r_e)^2}{2\alpha_0 r_e R_g}\left[\left(\frac{f}{KF_T}\right)^2 + \frac{1}{h_{FE}} + \frac{I_{co}}{I_E}\right]. \tag{7}$$

This has the general form

$$F = F_p\left(1 + \left(\frac{f}{f_c}\right)^2\right) \tag{8}$$

where f_c and F_p are as defined in Fig. 6.

The factor K that appears in (7) needs some explanation. Actually, noise figure depends upon f_α and not f_T. The reason for this is that noise voltages and currents appear simply as magnitudes in noise calculations. The frequency f_T determines gain and differs from f_α primarily because of the relatively large phase shift in h_{fe} compared to α. By definition, then, the factor K is

$$K \doteq \frac{f_\alpha}{f_T}. \tag{9}$$

The value of K depends upon the magnitude of the drift field in the base of the transistor, and is explained in detail in the section on characteristic frequencies. For most silicon transistors, $K = 1.2$.

Equation (7) does not include the effect of $1/f$ noise nor does it include the effect of parasitics, such as feedback capacity. Feedback capacity can reduce noise figure (as in the common-emitter connection) but gain is also reduced and the noise measure M[1] remains the same.

The importance of the dc common-emitter gain (h_{FE}) in noise figure (7) is often overlooked. For example, to obtain a noise figure of 1 dB or less at a frequency where

$$\left(\frac{f}{KF_T}\right)^2 \ll \frac{1}{h_{FE}}$$

h_{FE} must be greater than 100 for a typical transistor operated from a realistic source resistance. For modern planar devices, the shot noise from I_{co} is very small, and this term is often left out of (7).

B. Frequency Variation of Current Gain

1) Characteristic Frequencies: In the previous section it was pointed out that performance (i.e., gain and noise figure) both vary in the microwave region. This variation is due to the frequency dependence of a number of elements in the transistor. These in turn can best be characterized in terms of a number of characteristic or "cutoff" frequencies.

The gain of a common-emitter bipolar transistor is constant up to a "lower critical frequency" where it becomes conditionally stable. As frequency is further increased, it will become stable again at approximately $0.1 f_T$, and from there on the gain will continue to fall at approximately 6 dB per octave. For the gain to fall at exactly 6 dB per octave, the falloff in current gain would have to be the only frequency-dependent element in the transistor. This is not necessarily true. Near the limit of a transistor's usefulness where the gain is very low, gain may fall at less than 6 dB per octave due to capacitive feedthrough, or more due to other frequency-dependent elements.

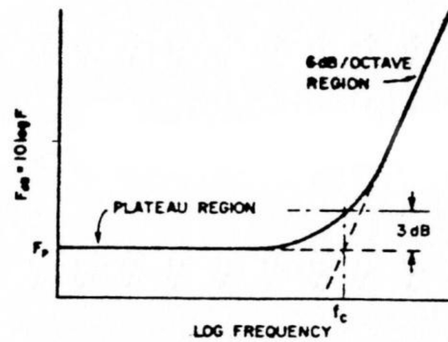

Fig. 6. Noise figure versus frequency.

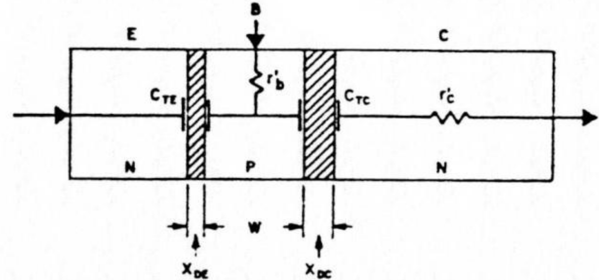

Fig. 7. One-dimensional view of a junction transistor.

The microwave range is in the 6-dB-per-octave region, and it is this frequency dependence that will now be examined. If a signal is put into the base or the emitter and taken out of the collector, it will encounter four successive principal regions of delay or attenuation. Fig. 7 shows these regions in a simplified cross-sectional view of a transistor. Since all silicon microwave transistors are presently n-p-n, the transistor is shown as such. Following the transit of carriers from the emitter we have, successively, the following.

1) The emitter–base transition capacity C_{TE} shunts the active emitter region.

2) Carriers must next cross the base region W through a combination of diffusion and electric field. During this transition the identity of a group of carriers will be lost and the signal attenuated.

3) Carriers next cross the collector depletion layer, X_{dc} wide, under the influence of an electric field (no diffusion).

4) If there is any appreciable resistance between the collector depletion-layer and the external collector terminal, a final RC delay is encountered.

Each of these elements can be regarded as a time delay.

$$\tau_{ec} = \tau_e + \tau_b + \tau_d + \tau_c. \tag{12}$$

- τ_{ec} total transit time emitter to collector
- τ_e emitter–base junction capacity charging time
- τ_b base transit time
- τ_d collector depletion-layer transit time
- τ_c collector-capacitance resistance charging time.

The time constants can be more conveniently expressed in terms

[1] Noise measure is defined as

$$M = G(F - 1)/(G - 1). \tag{10}$$

M was brought into use as a noise parameter since noise figure alone is a poor figure of merit in low-gain systems [7]. A somewhat more useful version of (10) is the noise figure of an infinite cascade of identical stages designated as F_∞,

$$F_\infty = M + 1 = F + (F - 1)/(G - 1). \tag{11}$$

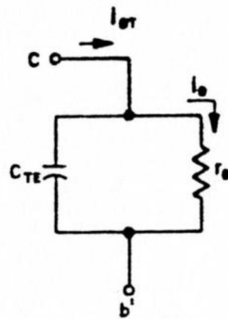

Fig. 8. Equivalent circuit of emitter-base junction.

of characteristic frequencies, as will be seen from the discussion that follows. Therefore, let

$$\tau = \frac{1}{\omega}. \tag{13}$$

Anticipating the following sections slightly we then obtain

$$\frac{1}{\omega_T} = \frac{1}{\omega_e} + \frac{1}{\omega_b} + \frac{1}{\omega_d} + \frac{1}{\omega_c}. \tag{14}$$

The frequency $\omega_T = 2\pi f_T$ is the most important parameter in a high-frequency transistor since it dominates both the gain and the noise performance (refer to Section I). Each of these characteristic frequencies will now be discussed.

a) The emitter–base junction cutoff frequency: When a transistor is operated in the normal mode, the emitter–base junction is in forward bias. The junction has a finite capacity associated with it as well as a resistance as shown in Fig. 8.

If a terminal emitter current i_{et} flows into the emitter terminal, it will divide between the capacitance C_{TE} and the resistance r_e. However, only the current that flows through r_e (sometimes called the space-charge resistance) gets injected into the base and is amplified. Thus the current in C_{TE} is a true parasitic. This is a simple RC-type cutoff so that

$$i_e = i_{et}\frac{1}{1 + j\omega r_e C_{TE}}. \tag{15}$$

The emitter current can now be normalized to the terminal current and called the high-frequency emitter injection efficiency γ_{hf}. Assuming that $\gamma_0 = 1$, at a cutoff frequency we shall define as ω_e,

$$\frac{|\gamma_{hf}|}{\gamma_0} = \frac{\sqrt{2}}{2}. \tag{16}$$

Thus from (15), (16)

$$\frac{1}{\omega_e} \cong r_e C_{TE}. \tag{17}$$

Equation (17) is valid for large devices but not for small-signal types intended for the gigahertz range. The collector capacitance C_{TC} must also be charged as well as some of the other miscellaneous capacitances such as those in the package. Therefore, (17) should be modified to give

$$\frac{1}{\omega_e} = r_e(C_{TE} + C_{TC} + C_X). \tag{17a}$$

b) Base transit characteristic frequency: The time for carriers to cross the base region is obtained by solving the transport equations [8], [9]. The solution is generally given in terms of β^*, called the base-transport factor. It is the ratio of current at the collector edge of the base to that at the emitter edge. β^* is complex since the carriers undergo a phase shift as well as a reduction in amplitude as they cross the base region.

If the carriers are first assumed to cross the base by diffusion alone, then

$$\beta^* = \operatorname{sech}\left[\frac{W}{L}(1 + j\omega\tau_B)^{\frac{1}{2}}\right] \tag{18}$$

where τ_B = lifetime for minority carriers in the base. At low frequencies, $\omega\tau_B \ll 1$ and

$$\beta^* = \beta_0^* \cong \operatorname{sech}\left(\frac{W}{L}\right). \tag{19}$$

β_0^* can be written as a truncated power series

$$\beta_0^* \approx 1 - \frac{1}{2}\left(\frac{W}{L}\right)^2 + \cdots \tag{20}$$

but $(W/L)^2$ must be much less than 1 for the transistor to be useful. Therefore, $\beta_0^* \approx 1$.

We now wish to obtain a suitable cutoff frequency. The frequency at which $|\beta^*|$ is 3 dB below its low-frequency value (which is ≈ 1) is designated as ω_β. Thus the magnitude of (18) must be obtained and set equal to $\sqrt{2}/2$ and solved for ω.

Before doing this is will be useful to make a slight transformation of the imaginary term in (18). The transit time across the base, t_B, can be written in terms of base width and diffusion constant:

$$t_B = \frac{W^2}{D}. \tag{21}$$

However, D is by definition

$$D = \frac{L^2}{\tau_B}. \tag{22}$$

Thus in (18) the imaginary (or frequency-dependent) term is $j\omega t_B$, where

$$t_B = \frac{W^2}{D} \tag{23}$$

or

$$t_B = \frac{W^2}{L^2}\tau_B. \tag{24}$$

Equation (18) then becomes

$$\beta^* = \operatorname{sech}\left[\left(\frac{W}{L}\right)^2 + j\omega t_B\right]^{\frac{1}{2}} \tag{25}$$

Equation (25) is then evaluated using a hyperbolic secant series to obtain $\omega_\beta t_B$ when $|\beta^*| = \sqrt{2}/2$. Using Pritchard's result [8], we obtain

$$\omega_\beta t_B = 2.43. \tag{26}$$

Substituting (24) into (26) gives

$$\omega_\beta\left(\frac{W^2}{D}\right) = 2.43 \tag{27}$$

or

$$\frac{1}{\omega_\beta} = \frac{W^2}{2.43D}. \tag{28}$$

The frequency ω_β is the frequency where the magnitude of the base transport factor is down 3 dB from its low-frequency value. If $\gamma_{bf} = 1$, it is also approximately equal to ω_α, the frequency where the common-base current gain is down 3 dB from its low-frequency value. ω_β is identical to $\omega_{\alpha i}$, the intrinsic (base only) cutoff frequency. A number of expressions for the frequency response of a transistor are written in terms of a characteristic frequency designated by ω_0. It is by definition

$$\frac{1}{\omega_0} \doteq \frac{W^2}{2D}. \tag{29}$$

Then

$$\omega_\beta = 1.2\,\omega_0. \tag{30}$$

There has been some confusion resulting from the similarity between (28) and (29), particularly since the solution of (25) using a hyperbolic cosine can lead to a factor of 2 instead of 2.43.

Equation (28) describes the cutoff frequency of the base transport factor for a transistor where the minority carriers move through the base by diffusion only. Carriers also can be caused to drift in the presence of an electric field, and even more important by a combination of field and diffusion [11]. The electric field in conventional planar transistors[2] is obtained through a grading of the impurities in the base [12], [13], i.e.,

$$\varepsilon = -\frac{kT}{q}\cdot\frac{1}{N(X)}\cdot\frac{dN(X)}{dX}. \tag{31}$$

An exponential distribution is a good approximation for $N(X)$ for diffused bases. The magnitude of the field obtained is then defined by a field factor η

$$\eta \doteq \ln\frac{N_{BE}}{N_{BC}}. \tag{32}$$

η can also be defined in terms of the electric field and the base width normalized to kT/q:

$$\eta = \frac{\varepsilon W}{\dfrac{kT}{q}}. \tag{33}$$

η can assume values of $\eta = 0$ (i.e., no field) to $\eta \cong 9$. The maximum value is set by other considerations in transistor design [13]. The effect of the electric field in reducing the transit time and raising the cutoff frequencies is described in a classic paper by Te Winkel [15]. This paper was written before the parameter f_T came into common usage, but it is quite apparent that f_T, as a new parameter, simplifies calculations a great deal.

The frequency[3] ω_{Ti} is greater than ω_0 when a drift field is present, and can be defined in terms of η and ω_0.

$$\omega_{Ti} = \omega_0\left[\frac{\frac{1}{2}\eta^2}{\eta - 1 + e^{-\eta}}\right] \tag{35}$$

which is useful for all but small values of η.

[2] This is not the only means of obtaining an aiding field in the base of a transistor. Long reported using a separate base electrode which was biased to produce an aiding field in the base of a transverse transistor [30].

[3] The frequency ω_{Ti} refers to the internal base characteristics, while ω_T is used to describe the terminal properties and may include the effect of other frequency-sensitive elements. If $\tau_{ec} \gtrsim \tau_e + \tau_b$, then ω_T is related to ω_{Ti} by

$$\frac{1}{\omega_T} \cong r_e C_{TE} + \frac{1}{\omega_{Ti}}. \tag{34}$$

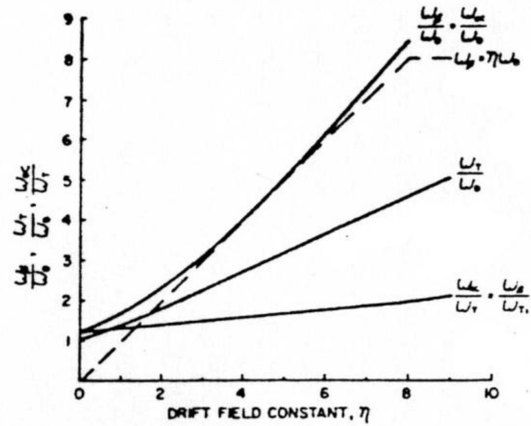

Fig. 9. Effect of drift field on characteristic frequencies.

The frequency ω_{Ti} has other interesting properties; at $\omega = \omega_{Ti}$, the magnitude of the internal common-emitter current gain = 1. The The presence of an aiding field affects the various cutoff frequencies as shown in Fig. 9. Note that ω_α and ω_β are more affected by the drift field than is ω_{Ti}. The frequency ω_{Ti}' is identical to ω_1 of Te Winkel [15]. Today ω_1 is usually used to designate the frequency where the *terminal* value of h_{fe} has dropped to one. It is usually higher than Te Winkel's because of capacitive feedthrough.

Since the presence of the drift field increases ω_α more than ω_{Ti}, the ratio of $\omega_\alpha/\omega_{Ti}$ also changes with η, i.e.,

$$\omega_\alpha = (1.21 + 0.09\eta)\omega_{Ti}. \tag{36}$$

Fig. 9 also shows the ratio of $\omega_\alpha/\omega_{Ti}$ as a function of η.

The frequency ω_α was at one time regarded as the principal high-frequency parameter. Since common-base operation was the only mode possible, this made some sense. Today, however, common-base operation is seldom used and ω_T is the dominant parameter. In fact, ω_α is only relevant as it applies to noise figure (refer to Section II-A).

A number of papers define τ_b (12) as $1/\omega_0$ and $\omega_b = \omega_0$. It is actually more rigorous to use ω_β instead of ω_0, since this is the actual cutoff frequency rather than a mathematically convenient time constant. Thus for a transistor with no drift field

$$\tau_b = \frac{1}{\omega_b} = \frac{W^2}{2.43D} \tag{37}$$

and for a transistor with a field [15]

$$\tau_b = \frac{1}{\omega_{Ti}} = \frac{W^2}{2D(0.8 + 0.46\eta)}. \tag{37a}$$

c) Collector depletion-layer transit time and characteristic frequency: The collector junction is operated in reverse bias when the transistor is normally used as an amplifier. Power devices can be driven into saturation (collector junction in forward bias) but the effect is unfortunate rather than planned. Because the junction is in reverse bias, there is a well-defined depletion layer, X_d wide. Although the junction is formed by diffusion in most microwave transistors, it has been found that the step-junction equations still apply and are simpler to use than those for graded junctions; therefore, in general,

$$X_d \cong \left[\frac{2\varepsilon\varepsilon_0(V + \phi)}{qN}\right]^{\frac{1}{2}} \tag{38}$$

or for silicon,

$$X_d|_{\mathrm{Si}} \cong 3.64 \times 10^3 \left[\frac{V + \phi}{N}\right]^{\frac{1}{2}} \text{ cm.} \tag{39}$$

For example, a typical silicon microwave transistor built on 5-Ω · cm (i.e., $N = 1.0 \times 10^{15}$) epitaxial material, and operated at 10 V, will have a depletion-layer width of about 3.6 μm. The field is then

$$\varepsilon = \frac{10.7}{3.6 \times 10^{-6}} = 3 \times 10^6 \text{ V/m.}$$

In spite of this very high field, carriers do not move through the depletion layer at the speed of light. At fields in the order of 1×10^6 V/m, the velocity in silicon saturates due to scattering effects at $V_{SL} \cong 8 \times 10^4$ m/s. The transit time across the depletion layer then becomes

$$\tau_m \approx \frac{X_d}{V_{SL}}. \tag{40}$$

The velocity V_{SL} is much greater than the equivalent velocity of carriers crossing the base region, and the time delay is insignificant in low-frequency devices. However, in microwave transistors, $X_d >> W$; as a result, for state-of-the-art devices,

$$\tau_m \cong \tau_b.$$

The expression given in (40) is not correct if the sinusoidal response of the depletion layer is required. To obtain this, Pritchard [8] defines a new parameter β_m, the depletion-layer transport factor, by

$$\beta_m = \frac{\text{current leaving the depletion layer}}{\text{current entering the depletion layer}}. \tag{41}$$

With the assumption that the collector multiplication is zero, the sinusoidal response is [8]

$$\beta_m \cong \left[1 - j\omega\frac{\tau_m}{2}\right]. \tag{42}$$

Since the depletion-layer transit time is a simple delay, it affects the transistor parameters by changing the transfer admittance Y_{21} to $\beta_m Y_{21}$. If the Y matrix is then evaluated for h_{21e}, it will be found that the denominator contains the term $\tau_m/2$ in addition to $1/\omega_\beta$ and the emitter–base charging time. We may then define ω_d as

$$\frac{1}{\omega_d} = \frac{\tau_m}{2} = \frac{X_d}{2V_{SL}} \tag{43}$$

also

$$X_d = K\left(\frac{V}{N}\right)^{\frac{1}{2}}$$

so that

$$\frac{1}{\omega_d} = \frac{K}{2V_{SL}}\left(\frac{V}{N}\right)^{\frac{1}{2}}. \tag{43a}$$

Early obtained the same results as (43) from a similar calculation [16].

d) Collector RC cutoff frequency: When transistors were first made, the substrate material was of a single resistivity. Thus to obtain reasonable breakdown voltages it was necessary that the entire substrate be in the order of 1–10 Ω · cm. As a result, there was a large high-resistivity region in the collector not covered by the collector depletion layer. The high-frequency resistance of this region is designated as r_c'. If a current is to flow out of the collector terminal, the collector capacitance must be charged through r_c'. This leads to a simple RC-type cutoff; thus

$$\frac{I_{c\,\mathrm{out}}}{I_{c\,\mathrm{in}}} = \frac{1}{1 + j\omega r_c' C_C} = \frac{1}{1 + j\dfrac{\omega}{\omega_c}} \tag{44}$$

where

$$\omega_c \doteq \frac{1}{r_c' C_C} \tag{45}$$

then

$$\tau_c = \frac{1}{\omega_c} = r_c' C_C. \tag{46}$$

Present-day microwave transistors are fabricated using a thin high-resistivity epitaxial layer on a lower resistivity substrate. In the structure, τ_c is usually negligible compared to the other three time constants in the transistor.

e) Summary: With the results obtained in the foregoing sections, we may now rewrite (14), using (17a), (37), (43), and (46). Common-emitter operation is also assumed.

For $\eta = 0$ (no field),

$$\frac{1}{\omega_T} = r_e(C_{TE} + C_C + C_X) + \frac{W^2}{2.43D} + \frac{X_d}{2V_{SL}} + r_c' C_C. \tag{47}$$

Or if a drift field is present and $\eta > 2.5$,

$$\frac{1}{\omega_T} = r_e(C_{TE} + C_C + C_X) + \frac{W^2}{2D(0.8 + 0.46\eta)} + \frac{X_d}{2V_{SL}} + r_c' C_C. \tag{48}$$

Table I summarizes the various characteristic frequencies discussed and how they are interrelated.

2) Behavior of Current Gain: The previous section develops certain characteristic frequencies that are related to the frequency limitations on current flow in the transistor. To complete the picture on active parameters, these frequencies will now be used to set up expressions for the current gain of the transistor.

The common-emitter current gain h_{fe} is the most important current gain parameter. It is intuitively easier, however, to first relate α to the characteristic frequencies already discussed. From α the common-emitter current gain can be derived. The parameter α is simply the ratio of the current leaving the collector to that entering the emitter:

$$\alpha \cong \gamma\beta^*\beta_m. \tag{49}$$

The emitter efficiency, like the base transport factor, has a low-frequency limiting value and a frequency-dependent term as well.

$$\gamma_0 \cong \frac{1}{1 + \dfrac{R_{EE}}{R_{BB}}}. \tag{50}$$

At high frequencies, γ_0 is reduced by the emitter transition capacitance.

$$\gamma_{hf} \cong \frac{\gamma_0}{1 + j\omega r_e C_{TE}}. \tag{51}$$

Equation (51) is actually a restatement of (15) in a slightly different form.

The base transport factor β^* (sometimes called the internal α) has already been discussed from the point of view of establishing its critical frequencies. The exact expression for α or β^* is long (see

TABLE I

Equation (1):	$\omega_0 \doteq \frac{2D}{W^2}$	a characteristic frequency appearing in the solution of the transport equations
Equation (2a):	$\omega_\beta = K\omega_0$	frequency where β^* is $\sqrt{2}/2$ of the low-frequency value
Equation (2b):	$\omega_\beta = 1.2\,\omega_0 = \frac{2.43D}{W^2}$	diffusion only, no drift field
Equation (2c):	$\omega_\beta = \omega_0 \frac{\frac{1}{2}\eta^2(1.21+0.09\eta)}{\eta - 1 + e^{-\eta}}$	general case where drift field is present $1.2\omega_0 \leq \omega_\beta \leq 8.1\omega_0$
Equation (3):	$\omega_a = \omega_\beta$	frequency where $\lvert\alpha\rvert$ is $\sqrt{2}/2$ of the low-frequency value, assuming $\gamma = 1$
Equation (4a):	$\omega_a = 1.2\,\omega_0$	no drift field
Equation (4b):	$\omega_a = \omega_0 \frac{\frac{1}{2}\eta^2(1.21+0.09\eta)}{\eta - 1 + e^{-\eta}}$	general case; see (2b) with drift field
Equation (5a):	$\omega_{Ti} = \alpha_0\omega_0 \cong \omega_0$	frequency where $\lvert h_{fe}\rvert$ is 1.0; diffusion only, no drift field
Equation (5b):	$\omega_{Ti} = \frac{\frac{1}{2}\eta^2}{\eta - 1 + e^{-\eta}}\,\omega_0$	general case with drift field
Equation (6a):	$\omega_\beta = \omega_a = (1.21 + 0.09\eta)\omega_{Ti}$	general case, including drift field
Equation (6b):	$\omega_\beta = \omega_a = 1.21\,\omega_{Ti}$	diffusion only, no drift field
Approximation 1:	$\omega_a \cong \omega_0$	only valid when $\eta = 0$
Approximation 2:	$\omega_a \cong \eta\omega_0$	only valid when $\eta > 2$
Approximation 3:	$\omega_{Ti} = \omega_0(0.8 + 0.46\eta) = \frac{2D}{W^2}(0.8 + 0.46\eta)$	only valid when $\eta > 2.5$

[15]) and too complex to give any insight into its behavior. A simpler approximation is given as

$$\beta^* = \alpha_i = \frac{\alpha_0 \exp\left[-j(0.22 + 0.098\eta)\right]\dfrac{\omega}{\omega_a}}{1 + j\dfrac{\omega}{\omega_a}}. \tag{52}$$

Since ω_a and ω_β are essentially identical, ω_β could also be used in (52). The term in the parenthesis on the right side of the equation is the so-called "excess phase" term and accounts for the additional phase shift caused by the field, if present. If no drift field is present, $\eta = 0$ and

$$\alpha_i\big|_{\eta=0} = \frac{\alpha_0 \exp\left[-j0.22\dfrac{\omega}{\omega_a}\right]}{1 + j\dfrac{\omega}{\omega_a}}. \tag{53}$$

The common-emitter current gain[4] h_{fe} is

$$h_{fe} = \frac{\alpha}{1 - \alpha}. \tag{54}$$

Also, from [15],

$$h_{fe} = \frac{\frac{1}{2}\eta^2}{\eta - 1 + e^{-\eta}}\,h_{fe0} \tag{55}$$

[4] The use of β for h_{fe} is avoided because β was used for the base transport efficiency.

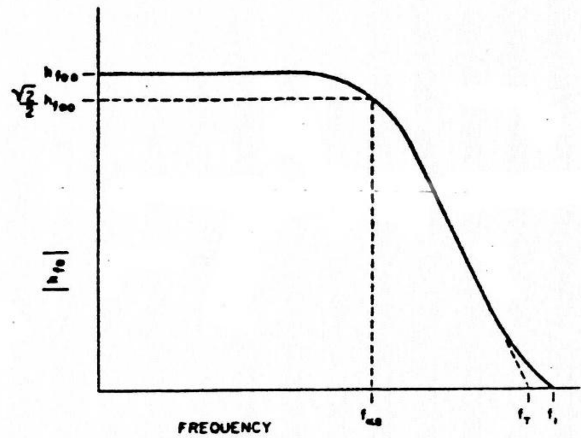

Fig. 10. Plot of $|h_{fe}|$ versus frequency.

which also can be written

$$h_{fe} \cong \frac{h_{fe0}}{1 + jh_{fe0}\left(\dfrac{\omega}{\omega_{Ti}}\right)}. \tag{56}$$

Equation (55) shows how the drift field influences h_{fe}, while (56) includes the effect by using ω_{Ti} as a frequency parameter. The magnitude of (56) is also useful.

$$|h_{fe}| \cong \frac{h_{fe0}}{\left[1 + (h_{fe0})^2\left(\dfrac{\omega}{\omega_{Ti}}\right)^2\right]^{\frac{1}{2}}}. \tag{57}$$

Fig. 10 is a plot of (57). If (57) is solved for the frequency where $|h_{fe}| = (h_{fe0})\sqrt{2}/2$ (which is called ω_{ae}), we obtain

$$\omega_{ae} = \frac{\omega_T}{h_{fe0}}. \tag{58}$$

It is interesting to note at this point that the presence of a drift field multiplies both ω_{Ti} and h_{fe0} by the same factor, thus the 3-dB cut-off frequency ω_{ae} is independent of the drift field [15].

Equations (56) and (57) can also be used with ω_T as well as with ω_{Tf}. If (57) is set equal to one and solved for ω, it will be found that ω equals ω_{Ti}. The *terminal* value of h_{fe} is altered by the effect of collector capacity and other parasitics as well, and will usually drop to one at a somewhat higher frequency. This frequency has now been designated as ω_1, the frequency where the terminal magnitude of h_{fe} actually becomes one. The same standard [17] also sets f_T as the frequency where the extrapolated value of $|h_{fe}| = 1$, with the requirement that the extrapolation is made from the region where $|h_{fe}|$ is falling at 6 dB per octave.

C. Parasitics

1) Base Resistance: The active or intrinsic transistor is confined to a small region under the emitter and extending across the base to the collector. It is customary to designate the intrinsic base as b' to differentiate from the external base b. The intrinsic base is a physically inaccessible region and cannot be contacted directly. As a result, there is a volume of resistive base material between the intrinsic base and the so-called base contact in a planar transistor (Fig. 11).

The current that flows in the base consists of 1) the α, or active current, which flows by diffusion, field, or a combination of the two; and 2) the $(1-\alpha)$ or "defect" current. The latter is a drift current and therefore attenuated by resistive losses.

Base resistance causes several undesirable effects:

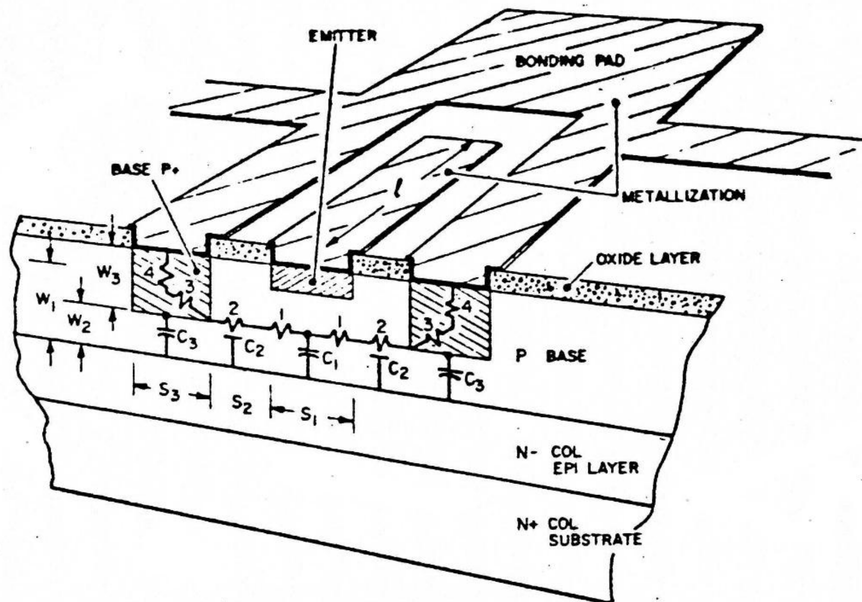

Fig. 11. Cross section of a planar transistor showing r_b' and capacitance. 1, 2, and 3 are parts of r_b', and 4 is R_c (contact resistance).

1) attenuation or loss signal in the base lead;
2) de-biasing of the region under the emitter (for example, the majority, or $(1-\alpha)$ current in an n-p-n transistor, biases the edges of the emitter positively with respect to the center of the emitter, causing the minority carriers (electrons) to concentrate near the edge; this also can be regarded as a form of feedback);
3) increased noise figure;
4) miscellaneous low-frequency effects, such as increase in saturated collector resistance, etc.

Because base resistance is a distributed and not a lumped resistance, it has been called the base "spreading" resistance. In a planar transistor, base resistance is really part of an RC transmission line. Fig. 11 shows a cross section of a modern microwave transistor, indicating that r_b' may be broken down into the following four regions:

1) base resistance under the emitter;
2) base resistance between the emitter and the p^+ region;
3) base resistance in the p^+ region itself;
4) contact resistance between the metal and the p^+ region.

Contact resistance is not properly a part of r_b', but from a circuit viewpoint, the effects on gain and noise are similar. Reference [18] shows how complex an equivalent circuit for the base region can be.

In early low-frequency devices, the capacitive reactances shunting r_b' were relatively high and r_b' was regarded as a frequency-independent element. This is not so in microwave transistors and certain other special types[5] where r_b' decreases with frequency due to capacitive shunting.

The calculation of base resistance from geometry is fairly straightforward if the resistivity and mobility are assumed constant throughout the base region under the emitter. When the impurity distribution is known, such as complementary error function, exponential, linear grade, or hyperbolic, the base sheet resistance can be calculated, and hence the base resistance [12]:

$$\frac{1}{R_{BB}} = q\mu \int_0^W N(X)\,dX \tag{59}$$

and

$$r_b' = \frac{R_{BB}}{W}. \tag{60}$$

The calculation of r_b' for more complex elements is given by Phillips [9]. A simple outline for estimating the low-frequency value of r_b' in a planar transistor is given here. (Refer to Fig. 11.)

$$r_{b1}' \text{ under the emitter: } \frac{\rho_1 S_1}{12 W l} = \frac{R_{BB1} S_1}{12 l},$$

$$r_{b2}' \text{ between the emitter and } p^+: \frac{\rho_2 S_2}{2 W_2 l} = \frac{R_{BB2} S_2}{2 l},$$

$$r_{b3}' \text{ in the } p^+: \frac{\rho_3 S_3}{12 W_3 l} = \frac{R_{BB3} S_3}{12 l}.$$

$$\text{Total } r_b' = \frac{1}{\text{number of emitters}} [r_{b1}' + r_{b2}' + r_{b3}' + R_c].$$

S_1, S_2, and S_3 are widths of the emitter, emitter-to-p^+ space, and the p^+ opening, respectively, as shown in Fig. 11.

Ordinarily mobility [μ in (59)] is considered constant in making an estimate of r_b'. Irwin has published graphs of the resistivity of diffused layers where mobility is changing with depth [19]. His curves cover coerror functions and hyperbolic distributions in silicon.

Some recent data seem to indicate that very shallow junctions do not follow accurately in any of the impurity distributions usually described in the literature. The estimate of r_b' obtained as shown in Fig. 11 is still of considerable value in the design of a microwave transistor.

2) *Capacitance:* As would be expected, the internal capacitances of a transistor play an important role in the frequency response of the device as an amplifier. Extrinsic capacitances, such as those in the bonding pads and package, also affect performance. Those in the device itself will be considered first.

The active portion of a transistor has two types of capacitance, transition and diffusion, both of which are associated with the two junctions.

a) Emitter–base junction capacitance:

1) Transition capacitance C_{TE} arises from the fact that the

[5] The 2N929-930 type has an extremely lightly doped base region to enhance h_{fe}. Base resistance is 750–1000 Ω at dc and about 200 Ω at 200 MHz.

emitter has a finite area and a depletion layer. Since the silicon transistor junction is formed by diffusion and graded to some degree, it shows a 1/3-power voltage dependence when measured under reverse bias conditions. However, the emitter–base junction is normally operated in forward bias, and under this condition the step- (or 1/2-power) junction equations apply. The step-junction equation is simpler to handle:

$$C_{TE} \cong A_E \left[\frac{\varepsilon\varepsilon_0 q N_{BE}}{2(V+\phi)}\right]^{\frac{1}{2}} \tag{61}$$

or for silicon

$$C_{TE} \cong A_E \times 4.12 \times 10^3 \left(\frac{N_{BE}}{V+\phi}\right)^{\frac{1}{2}}. \tag{62}$$

For a typical silicon microwave transistor the contact potential ϕ is approximately 0.7 V. The applied voltage V is positive when the device is in forward bias. In other words, forward bias reduces the total voltage and increases C_{TE}.

If, for design purposes, it is desired that C_{TE} be reduced, only the emitter area A_E can be changed without significantly affecting the other parameters. The relative dielectric constant ε is set by the material used and N_{BE} is usually determined by other considerations, such as r_b' and h_{fe}. Occasionally N_{BE} can be reduced to reduce C_{TE} provided the emitter width is also narrowed to keep r_b' from increasing.

Since C_{TE} is shunted by r_e, the space-charge resistance of the emitter, and C_{DE}, the diffusion capacitance, it cannot be measured directly under forward bias. It is usually inferred from a plot of $1/I_E$ versus $1/f_T$ (refer to measurements).

2) Regarding the diffusion capacitance C_{DE}, when an ac voltage is applied to the forward biased emitter—base junction, the injected charge in the base is modulated. This change in charge with voltage defines a capacitance C_{DE}:

$$C_{DE} \doteq \frac{\Delta q_B}{\Delta V_{BE}}. \tag{63}$$

This equation can be manipulated to give C_{DE} in terms of base width and the diffusion constant:

$$C_{DE} = \frac{1}{r_e}\left(\frac{W^2}{2D_B}\right). \tag{64}$$

The expression in the parenthesis has the dimensions of $1/\omega$ and is characteristic base frequency, as defined in the section on characteristic frequencies. Therefore,

$$C_{DE} = \frac{1}{r_e\omega_0} = \frac{qI_E}{kT}\cdot\frac{1}{\omega_0} \tag{65}$$

which is correct for a transistor where the carrier is moved by diffusion only. In the case where there is a drift field, ω_{Ti} must be substituted for ω_0:

$$C_{DE} = \frac{1}{r_e\omega_{Ti}}. \tag{65a}$$

Since $\omega_{Ti} > \omega_0$, it can be said that drift field reduces C_{DE} in the same proportion that it increases ω_{Ti} over ω_0. At medium and higher currents, C_{DE} tends to mask out C_{TE} because C_{DE} varies directly with emitter current (64).

b) Collector–base junction capacitance: In this section it will be necessary to refer to the physical cross section of a planar transistor (Fig. 11) in order to differentiate the various capacitances. The base consists of three major regions: one under the emitter, one between the base and p^+, and one associated with the p^+ itself. The capacitances associated with these regions where they form a junction with a collector are in the form of an RC transmission line. A rigorously accurate representation of this region can result in a very complex equivalent circuit [18]. For the purposes of this paper, two or three regions will be sufficient. The part under the emitter is most important and it is C_1 (Fig. 11) that should be used in (2) in the expression for gain. Often the collector capacitance is arbitrarily divided into an inner and an outer region designated as C_{CI} and C_{CO} where $C_{CI} = C_1$ and $C_{CO} = C_2 + C_3$.

As in the emitter–base junction there is both a transition capacity and a diffusion capacity associated with the junction. For collector diffusion capacity to be present, the base width must modulate with changes in collector voltage. Diffusion capacity is significant in alloy transistors where the collector is metallic, and the depletion layer lies almost entirely in the base region. The situation is quite different in a silicon microwave transistor where $N_{BC} > N_C$. Hence, the depletion layer lies almost entirely in the collector epitaxial region and the base width does not change significantly with collector voltage except near saturation conditions [20], [21].

The total value of C_{TC} for a silicon transistor can be written as

$$C_{TC}\Big|_{\text{total}} = A_{c_{\text{cm}^2}}(4.12 \times 10^3)\left(\frac{N_C}{V+\phi}\right)^{\frac{1}{2}} \tag{66}$$

where N_C is the impurity density in the collector epitaxial region. Epitaxial material is generally specified in terms of resistivity ρ rather than impurity density. The relationship between ρ and N is

$$\rho = \frac{1}{q\mu N}. \tag{67}$$

Mobility μ is fairly constant for values of ρ between 1 and 10 $\Omega\cdot$cm. Then for n-type silicon,

$$\rho \cong \frac{5.1 \times 10^{15}}{N} \tag{68}$$

which can be substituted in (66) to give

$$C_{TC}\ \text{total} = \frac{A_{\text{cm}^2} \times 2.94 \times 10^{11}}{[\rho(V+\phi)]^{\frac{1}{2}}}. \tag{66a}$$

An estimate of the fractional values for the various portions of C_{TC} (i.e., C_1, C_2, and C_3 in Fig. 11) is made by taking proportions by area. The value of C_{CI} is 20 to 25 percent of the C_{TC} total as shown in the figure. In the past it was a practice to measure the collector base time constant $r_b C_{CI}$ and r_b'; and from these two measurements a value of C_{CI} could be inferred. For the older mesa transistor this was reasonably accurate, but now the collector base time constant itself is complex (see measurements and modeling) and this method is no longer valid. Also, the fact that at low frequencies Im $(Y_{22E}) \cong j\omega C_{CI}$ and Im $(h_{22e}) \cong j\omega(C_{CO} + C_{CI})$ can be used to separate C_C into its components.

Fig. 11 also shows the bonding pad used to connect the base of the transistor to the outside world. It forms a capacitance with the collector region which lies underneath it. The dielectric in this case is silicon dioxide, silicon nitride, or a combination of the two. Also the oxide may be a combination of grown and deposited material. The dielectric constant will vary then with the type of dielectric and how it was treated after it was formed. The thickness of this layer is usually not very great, in the order of 2000 to 10 000 Å. It is also the practice to minimize the pad area in order to keep down the pad capacitance. A typical value for pad capacitance is in the order of 0.05–0.1 pF/mil².

The pad and package capacitances lie outside of any significant loss resistance and therefore affect bandwidth but not the intrinsic

device gain. "Extrinsic" capacitances such as those between collector and base do reduce common-emitter gain, but theoretically can be neutralized. However, wide-band neutralization at microwave frequencies is very difficult, and good transistor design will be such as to minimize bonding pad and other parasitic capacitance.

D. Transistor Modeling

This section will briefly describe equivalent circuits or models as applied to microwave transistors. In general, models tend to fall into three categories: device, measurement, or circuit oriented. The parameters derived from these models are often similar, and certain figures of merit such as the maximum stable gain have exact counterparts in the different systems.

Fig. 12(a) is an example of a device-oriented model because most of its elements have direct physical counterparts in the real transistor. The frequency dependence of this model, except for the effect of C_{TE}, is implied in the expression that must be used for the α current generator. While not shown in this figure, the addition of direct capacitances between all three terminals and inductances would improve the accuracy somewhat.

The T equivalent model is particularly useful because it can be used for noise calculations by simply adding the appropriate noise voltage or current generators (refer to Fig. 5).

Another approach to this type of model is the hybrid π shown in Fig. 12(b). The frequency dependence of the output current generator is eliminated by adding the diffusion capacity to the emitter–base emittance, where

$$C_{DE} = \frac{1}{\omega_{Ti} r_e}.$$

Note that this is a common-emitter circuit and consequently r_e is divided by $(1-\alpha_0)$. This model readily yields the usual approximations to the h parameters [8], [9]. For example, at low frequencies

$$h_{11e} = r_b' + \frac{r_e}{1-\alpha_0} \tag{69}$$

and therefore, if $\alpha_0 \cong 1$,

$$h_{11e} \cong r_b' + h_{fe0} r_e \tag{70}$$

or at high frequencies, when $C_{DE} \gg C_{TE}$,

$$h_{11e} \cong r_b + \frac{1}{\dfrac{1-\alpha_0}{r_e} + \dfrac{\omega}{\omega_{Ti} r_e}}$$

and if $(1-\alpha_0) \ll \omega/\omega_{Ti}$,

$$h_{11e}\Big|_{hf} \cong r_b' + r_e\left(\frac{\omega_{Ti}}{\omega}\right). \tag{71}$$

A measurement-oriented model is usually based on considerations of accuracy and ease of measurement at a particular band of frequencies. As the transistor evolved and became applicable to higher and higher frequencies, the system of measurements also changed. Early transistors were usually characterized by the hybrid parameters; later systems used Y parameters, while today scattering parameters are most popular. In the microwave range it is difficult to realize an effective short or open circuit and thus S parameters are based on nominal and such easily achievable terminations as 50 Ω. The present popularity in scattering parameters is also due to the availability of accurate and easy-to-use measuring equipment. Some of the scattering parameters have a direct relationship to performance in a real system. For example, the 50-Ω insertion-power gain is $|S_{21}|^2$. The equivalent circuit [Fig. 12(c)] is very simple.

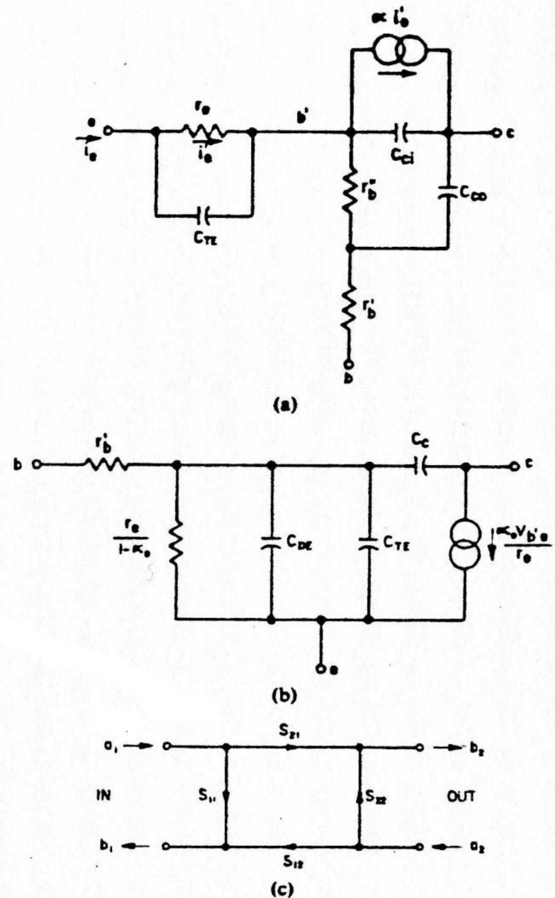

Fig. 12. (a) T equivalent circuit. (b) Hybrid equivalent circuit. (c) Scattering parameter equivalent circuit.

Parameters a_1, b_1, etc., are waves entering or leaving the terminals and have the dimensions of the square root of power. Several excellent references on the scattering matrix are available [22]. Scattering parameters are most useful for circuit design but are very poor as an adjunct to transistor design since they do not relate easily to intrinsic device parameters. The (ABCD) matrix is a model that is adapted to the cascading of stages. This is an example of a circuit-oriented model. The parameters are usually obtained by transformation from another model, such as the scattering parameters.

III. Transistor Design and Fabrication

This section will describe briefly the most important steps in the design–fabrication cycle. In order to keep the size of the section tractable, techniques not specifically characteristic of microwave transistors will be given only brief mention. Other details like clean-up procedures will be left out completely. Fig. 13 is an outline covering the main steps.

A. Selection of Geometry

Within the limitations of a given technology a designer should attempt to make a device that will meet the exact design goals as closely as possible. Over design would result in a device that would be uneconomical and probably unstable at the frequency of application. Thus a design using the maximum possible f_T and the minimal possible geometry should be avoided, except where actually needed to meet performance goals.

For a power transistor, the objective power, efficiency, and operating voltage are used to obtain an average current. From this the emitter periphery can be calculated, using 1.5 mA/mil as a first-order estimate. Typical emitter widths for competitive devices are approximately

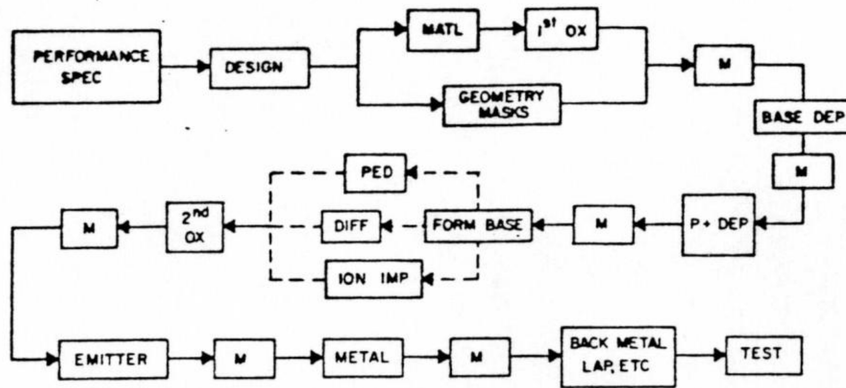

Fig. 13. Process flow for silicon microwave transistors (simplified). *M* is photomasking.

1.0 GHz	0.2 mil
1–2 GHz	0.1 mil
2–4 GHz	0.07 mil
4–6 GHz	0.05 mil.

The length-to-width ratio of an emitter should not exceed about a 20-to-1 ratio to minimize the voltage-drop down the finger. The physical arrangement of the emitters (i.e., device aspect ratio) should be determined from the thermal resistance versus ease of fabrication considerations. Long devices have lower thermal resistance but also lower fabrication yields.

A small-signal transistor design will be approached somewhat differently. Using the noise figure (7) together with an estimate of the f_T, which can be obtained, a value for r_b' is calculated. The base sheet resistance required for estimating f_T is usually already known, and thus r_b' can be used to obtain an emitter width and spacing (refer to Section II-C).

The p^+ area (Fig. 11) must be determined next. Its width is based on the contact resistance that is realizable with the metal system to be used. Contact resistance is usually expressed in $\Omega \cdot cm^2$. Hooper *et al.* [23] published data on contact resistance versus base impurity concentration for molybdenum. Fujinuma [24] reported values for platinum silicide somewhat lower than those for molybdenum.

The width of the p^+ region with a metal system must then be selected to give a contact resistance at least as low as r_b' and preferably lower. A wide p^+ region lowers contact resistance and makes photomasking easier, but adds to the transistor collector capacity.

Once the configuration of the p^+ and emitters has been determined, the basic geometrical design is set. Contact pads should be made 1 mil square or even less, when multiple pads must be used to handle the current. For very small transistors, with active areas less than 1 square mil, the pads should be less than 0.25 mil^2. Pad capacity is also minimized by using a relatively thick oxide.

B. Material

Because of the very shallow junctions used, the breakdown voltage of microwave transistors is almost always determined by the radius of curvature at the edge of the base [25]. This limitation can be circumvented to some degree by including a guard ring as a part of the p^+ structure and driving it in much deeper than the active base under the emitter. Mesa etching could theoretically provide a usable increase in breakdown voltage if the edges of the mesa could be passivated effectively. Microwave transistors are further limited in selection of material by the collector capacitance (66) versus depletion-layer transit time (43a) tradeoff. It is usually resolved by taking the overall required terminal f_T and breaking it down into the base and collector depletion-layer transit times. With the collector-depletion-layer transit time and the operating voltage known, the resistivity of the epitaxial layer can be determined. The thickness of the layer must be somewhat greater than the depletion layer or C_C will be higher than calculated. A good design will seek a reasonable proportion between τ_b and τ_d. An obviously poor design might have a low base cutoff frequency and a high depletion-layer cutoff frequency. Such a device would have a relatively high collector capacity and a low gain.

If a transistor is to deliver a substantial amount of power, the resistivity of the epitaxial region must be lower than that for an equivalent small-signal transistor. Power output is inversely proportional to r_c' and to the resistance of the column of material with a cross-sectional area equal to the emitter area and length equal to that of the epitaxial layer thickness,

$$P_{out} \propto \frac{l}{r_c'} \propto \frac{A_e}{t_{epi}\rho_{epi}}. \tag{72}$$

Present-day microwave transistors are usually built on 0.25-to-5-$\Omega \cdot$ cm material. Power devices have a p^+ depth that yields a breakdown voltage in the order of 35 to 50 V. Small-signal transistors usually have a lower breakdown voltage (≈ 20 V), usually because of the shallower diffusions used. State-of-the-art high-f_T (>7 GHz) transistors are built on 0.25–1-$\Omega \cdot$ cm epitaxial material in order to keep the collector depletion layer narrow. When this is done, epitaxial layer is operated only partially depleted.

C. Base Formation

Following the first oxide, the base area is opened up and deposited. After depositing the p^+ part of the base, the entire base region can be diffused. The primary base will have a higher (up to 1500 $\Omega/\square$) sheet resistance in order to minimize emitter dip effect (i.e., enhanced diffusion boron under the emitter) and to keep mobility high.

Alternately, the primary base can be implanted [26], [27], or first deposited, and then the actual diffusion accomplished through the bombardment with protons [28].

D. Emitter

Following the base formation, a second oxide is deposited on the slice. This oxide is generally of the type formed by the thermal decomposition of a gas or liquid. It is a low-temperature process so as to minimize the possibility of driving in the base farther. The emitter is then defined and diffused. Emitter diffusion times tend to be very short for microwave transistors compared to the hours used for low-frequency transistors. The temperatures are also low, generally less than 950°C.

E. Impurity Profiles

It is useful to plot the concentration of impurities in the wafer as a function of the distance from the surface. Since the impurities are introduced from the surface, the concentrations are highest there (with the exception of the implanted devices). Plots typically show the concentration at an emitter site, although plots can also be made starting in the p^+ region. An impurity plot can show the impurity concentration by type or sign or the net concentration, i.e., $|N_D - N_A|$. The net concentration shows which type of impurity predominates, as well as giving some indication of the base resistance.

Fig. 14(a) is a plot of the impurity concentration versus depth for an ideal device, and a diffused base with two types of emitters. To keep the comparison meaningful, the base width W has been kept constant. The "ideal" emitter has a concentration that is constant and close to solid solubility. The ideal base is also rectangular and extends from X_e to X_b below the surface. This base is ideal from the viewpoint of minimizing base resistance only. Some grading would be useful if f_T were the parameter to be optimized.

The boron or base impurities (designated as N_b) extend into the base to where they equal the epitaxial layer impurity level N_C at the base depth X_b. The base width is in the order of 0.10–0.2 μm for state-of-the-art devices.

The emitter impurities are shown for two types of dopants, phosphorous and arsenic. Phosphorous usually produces a higher surface concentration (N at $X = 0$), but has a much less abrupt profile compared to arsenic. The arsenic profile is best for at least three reasons.

1) There is less compensation in the base region, and therefore r_b' is lower. Compensation means that where there are equal quantities of donors and acceptors, the impurities are thus neutralized and cannot transport current. The shaded area in Fig. 14 is this region.

2) Emitter push effect is eliminated, and narrower bases (higher f_T) are obtainable.

3) In the region of compensation, the base impurities have a negative grading, i.e., they increase with depth, resulting in a retarding field. It is thought that this retarding field cancels the effect of the aiding field in the remainder of the base resulting in what is essentially a "diffusion" transistor. The only silicon transistor that exhibits a net positive drift field also has both an implanted base and an arsenic emitter [26]. It is uncertain at this time which of these was responsible for the presence of the drift field.

The originally grown junction transistors had the impurities added during the growing of the crystal. When the diffused base or mesa transistor first appeared, the doping was added by diffusion, usually in a quartz tube at an elevated temperature. Now with the use of an accelerator, impurities may be implanted or caused to diffuse into the crystal by radiation.

Implantation [Fig. 14(b)] is unique in that it can place the impurities so that the peak of the distribution (which is Gaussian) is below the surface. Because the distribution can be controlled to some degree by controlling the energy of the ions, a more "rectangular" profile with lower base resistance and less retarding field can be obtained. Ion implantation, however, has some very serious disadvantages.

1) Because the relatively large boron ions damage the crystal during the radiation process, the slice must be annealed at a temperature close to that at which diffusion occurs. Annealing temperatures of 600–700°C are typical.

2) Even after annealing, a relatively large part of the boron impurities are tied up in Frenkel pairs, which are inactive and are not available to carry current.

3) When the emitter is diffused, the emitter impurities should intersect the peak of the base impurities. The emitter diffusion is very

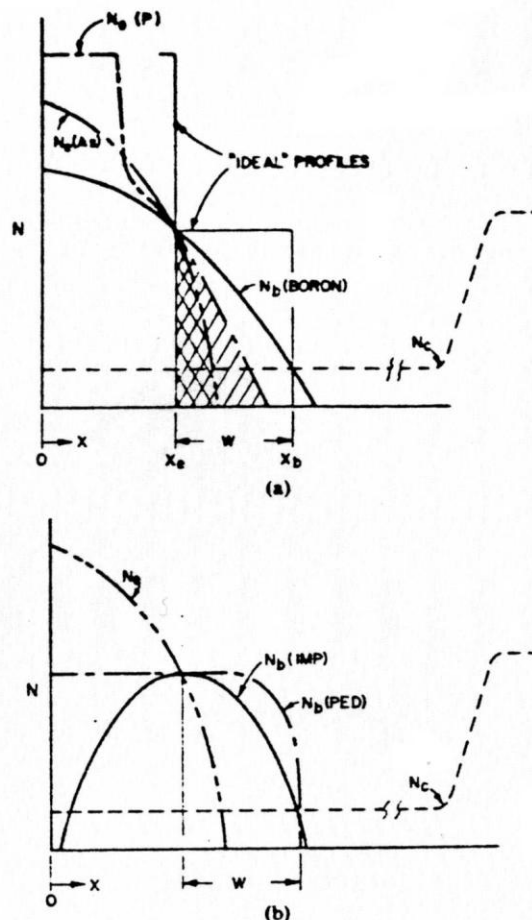

Fig. 14. (a) Comparison of arsenic and boron emitter profiles. (b) Comparison of impurity profiles obtained by ion implantation and proton enhanced diffusion.

critical since diffusions too shallow or too deep can result in no transistor action at all.

Proton enhanced diffusion (PED) appears to offer some advantages over both diffusion and ion implantation. PED uses the relatively small nuclei of the hydrogen atom to generate vacancies in the crystal. The process includes deposition of the impurity (e.g., boron) on the surface of the slice followed by bombardment with protons at a temperature in the 400–700°C range. The boron atoms quickly diffuse into the crystal to a depth accurately determined by the energy of the protons. Fig. 14(b) indicates that the diffusion front could be close to ideal. Compared to the implanted profile, there is more compensation in the emitter, but this does not appear to be a serious drawback. A comparison of the diffused and PED transistor profiles with the same base width showed a reduction in r_b' of about 1.8 to 1 for the PED device.

F. Contacts

The slice is again photomasked and the reverse contact mask is used to open up the base contact areas. A number of contact systems are suitable for microwave transistors. Aluminum in general is not suitable because of the difficulty in obtaining clean shallow junctions. Systems based on the following metals have been used successfully on a variety of microwave devices: contacting metals (Al, Mo, Ni, Cr, Ti, PtSi); barrier metals (W, Mo, Pt); and top metals (Al, Au). When platinum silicide is used, the platinum must be deposited first and the silicide formed either during the deposition process or by the subsequent heat treatment. Silicide will form only in the contact opening over the bare silicon and the remainder of the platinum can be removed chemically. The refractory metal is deposited next and

then the gold. An electron gun or sputtering is used in the deposition of the refractory metal.

Sputtering of the metal results in a contact that adheres well, but excessive heat can cause sufficient damage to make the dc current gain of the device quite low. After photographically defining the contacts, the transistor is ready for the final processing.

G. Final Processing

These steps are essentially the same as for lower frequency transistors. Slices are normally processed at about a 0.01-in thickness. During the processing, the back becomes contaminated so that it is later lapped off to a final thickness of approximately 0.005 in. For high-power transistors, the final lapping has an additional benefit in that it reduces the thermal resistance of the die. After lapping, the slice may or may not be gold backed depending upon the die attachment system used. Backside gold is usually doped with phosphorous to insure that the metal semiconductor interface is nonrectifying, i.e., the n-type dopant on the n substrate will not produce an unwanted junction. The slice is then diced in the usual manner and is ready for packaging.

H. Other Variations

Conventional photomasking, which uses 3000–4000-Å light, has a limitation due to interference effects. This limit is in the order of 1.0 μm. An electron beam is now being used to define the geometry of smaller elements (for example, the emitter stripes). The beam is guided electronically, or the slice is moved mechanically, to trace out the desired pattern. Electron beam definition can probably be extended to give lines of less than 0.10 μm. Fig. 13 summarizes the process flow for a silicon planar microwave transistor.

I. Packaging

Transistors have conventionally been supplied in packages to protect the die and to increase the size of the unit so that a typical user can handle it conveniently. At the higher frequencies (i.e., >4 GHz), it is becoming apparent that conventional packaging will not be practical, and the die must be mounted directly in a microwave integrated circuit. For example, a chip mounted in the 0.07-in package will give 1 dB more gain at 4 GHz than it will in a package twice the size, but even then the chip parameters are measurably degraded by the smaller package. The main reason for this degradation is that the sealing system must occupy a physical space that separates the chip from the external circuit. This separation results in an increased lead inductance that reduces gain and bandwidth. The physical configuration of the package influences this loss to some extent and a coaxial package will perform slightly better. However, the coaxial package does not lend itself well to other than coaxial circuitry, while the trend today is more and more to microstrip.

Microwave transistor packages, where they can be used, should give adequate protection from the environment in which they are to be used. As a package is made smaller it becomes increasingly difficult to obtain a reliable hermetic seal. Three sealing technologies are presently in use: glass-to-metal, ceramic-to-metal, and plastic. Of the two hermetic systems, a glass-to-metal seal is the easier to realize, but it is also the more fragile. Ceramic-to-metal seals rely on a sophisticated brazing technique and are somewhat more expensive to build, but are superior mechanically. A package built using the latter technique is shown in Fig. 15(c). Plastic seals are economical but nonhermetic and, in addition, degrade the characteristics of higher frequency transistors. The loss in gain suffered at these higher frequencies in a small-signal transistor seems to be due more to increased capacity than to the losses in the potting dielectric. A new sealing technique, where the seals are sandwiched into the uncured ceramic or brazed into slots in the ceramic, gives promise of a more rugged package for small-signal applications.

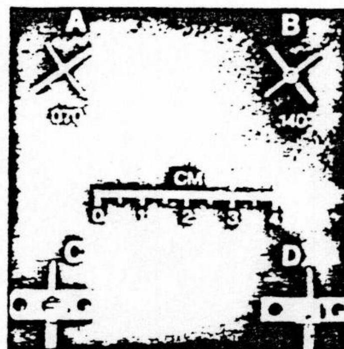

Fig. 15. Microwave transistor packages. *A* and *B* are small signal, and *C* and *D* are power. (Courtesy Ceradyne, Inc.)

TABLE II

Material	Approximate Thermal Conductivity (cal cm^{-1}°C^{-1})
BeO	0.56
Cu	0.97
Al_2O_3	0.045
Glass	0.002
Si	0.24–0.35
Diamond	1.51

If there is sufficient dissipation within the transistor to raise the temperature of the chip over 125°C, the package design must also include means of dissipating the heat. The thermal resistance θ of a package is usually given in °C/W; thus

$$T_j = T_s + P_D\theta. \tag{73}$$

A junction temperature T_j of 125°C is now considered a good number for a high-reliability system. The thermal resistance θ will include the resistance in the chip itself plus that of the package, and any other resistance in the heat path to the final sink which is at T_s.

Most circuit applications require that the collector be isolated from the ground plane, which means that the package must include an insulator. Beryllium oxide (BeO) is the most commonly used material. Table II gives a short list of the thermal characteristics of several materials. It shows why BeO is preferred to Al_2O_3 and why diamond is regarded as the ultimate in an insulating heat sink. Present-day power devices are thermally limited by the resistance of the chip itself. Most of the dissipation in a transistor takes place in the collector depletion layer. This is less than 1 μ from the upper surface, while the die thickness is in the order of 75–125 μm. It is difficult to thin chips to less than 50 μm, and the handling and assembly problems are multiplied. An inverted mounting technique, such as used for avalanche diodes, will be the ultimate approach to minimizing thermal resistance in transistors. A reliable system for separating the emitter and base contacts is the biggest obstacle yet to be overcome before inverted mounting will become practical. There is a further benefit to this type of mounting if the emitter is made the common element. The advantage is that the common lead inductance will also be reduced with the result that stability and gain are both improved.

IV. Measurements

This section will be concerned primarily with measurements that are used to determine basic parameters and control the fabrication process. Noise figure measurement would usually be considered a

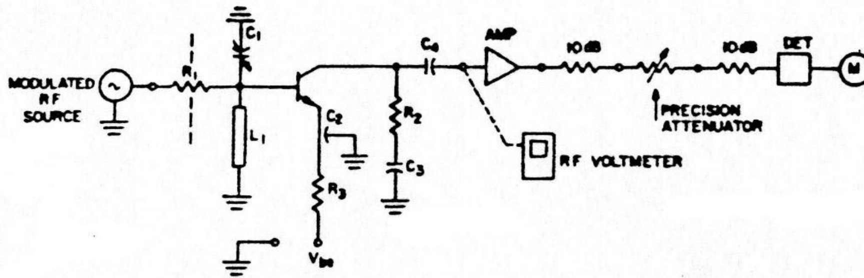

Fig. 16. Test setup for measuring f_T. Here $R_1 \cong 10$ kΩ; $R_3 = V_{bb}/I_E$; $R_2 = 1$ Ω; $C_1 = 0.5$–5 pF; C_2, $C_3 = 0.05$ μF; and $C_4 = 0.001$ μF.

performance criterion, except that for microwave transistors it is the only means of obtaining values for certain parameters. The measurements discussed here are an important part of the information "feedback loop" in transistor design. The discussion will include measurement of f_T, f_a, η, r_b', C_C, ρ_{epi}, C_{TE}, and $r_b'C_C$.

A. Measurement of f_T.

In the section on current gain it was pointed out that f_T is an extrapolated parameter [17] obtained by measuring $|h_{fe}|$ in the 6-dB-per-octave falloff region, i.e.,

$$f_T = f_{test}|h_{fe}| \tag{74}$$

where $|h_{fe}|$ is obtained at the test frequency. The first step in the measurement of f_T is to determine a proper test frequency so that [17]

$$2 < |h_{fe}| < 10.$$

If the approximate value of f_T is not known, the test frequency must be obtained by trial and error. The validity of a measurement is checked by changing the frequency by one octave and looking for a 6-dB change in $|h_{fe}|$.

For most microwave transistors, a suitable f_T test frequency is in the range of 400–1000 MHz. If measurements are made only occasionally a transfer bridge (GR 1607A) can be used. However, if f_T must be monitored continuously, two other alternatives are possible. The first is to measure the scattering parameters and then from these calculate $|h_{fe}|$, where

$$h_{fe} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}. \tag{75}$$

The calculation is not simple and is best done using a computer. It is also possible to measure $|h_{fe}|$ directly using a special text fixture. A suitable setup for 400 MHz is shown in Fig. 16.

C_1 and L_1 are used to tune out the package and fixture input capacity. R_1 is the constant current source. It is made by evaporating tantalum on a 0.140- by 1.00-in ceramic rod and anodizing it to the desired resistance. For 1 percent accuracy,

$$R_1 \geq 100\left[|h_{fe}|\frac{0.026}{I_E} + r_b'\right]. \tag{76}$$

The resistor R_2 is a 1-Ω disk or several chip resistors in parallel. Note that the system shown uses an AM-modulated 400-MHz test signal. This makes possible a very small input test current into the transistor itself. An RF voltmeter can also be used, but sensitivity may be a problem.

B. Measurements of f_a

This parameter is not directly accessible in microwave transistors because the terminal value of α may never drop to $\sqrt{2}/2$ due to parasitics. However, f_a can be obtained from a noise figure plot. Fig. 6 shows how the corner frequency f_c is obtained. From this and (77), f_a is obtained.

$$f_a = \left[\frac{Kf_c^2}{1 + \frac{r_b'}{R_g} + \frac{r_e}{2R_g} + \frac{K}{h_{FE}}}\right]^{\frac{1}{2}} \tag{77}$$

where

$$K = \frac{(R_g + r_b' + r_e)^2}{2\alpha_0 r_e R_g}. \tag{78}$$

C. Measurement of η

This parameter is the drift field factor and, like f_a, must be inferred from noise measurements. First, f_T and f_a are obtained as outlined in Sections IV-A and B. Referring to (35) we obtain

$$\eta = \left[\frac{f_a}{f_T} - 1.21\right]11.1. \tag{79}$$

D. Measurement of r_b'

The classical method of obtaining base resistance was simply to measure h_{11} at a relatively high current and frequency, i.e.,

$$h_{11e} \cong r_b' + \frac{0.026}{I_E}\frac{\omega_T}{\omega}. \tag{71}$$

If I_E is large,

$$h_{11e} \cong r_b'. \tag{80}$$

This is again a case of the older method no longer being usable. If the second term on the right-hand side of (71) is to be negligible, then the test frequency must be in the gigahertz range. As a result h_{11e} becomes very complex. A more accurate expression is then

$$h_{11e} = r_b' + \omega L_b + \frac{\omega_T}{\omega}\frac{0.026}{I_E} + \omega_T L_e. \tag{81}$$

Thus the measurement of h_{11e} is not a useful approach to obtaining r_b' in a modern microwave transistor.

Referring to the noise figure expression (7), let

$$\frac{I_{c0}}{I_E} \ll \left(\frac{f}{f_a}\right)^2 \ll \frac{1}{h_{FE}}$$

and

$$\alpha_0 \cong 1.$$

Under these assumptions, the plateau frequency noise figure F_p is

$$F_p = 1 + \frac{r_b'}{R_g} + \frac{r_e}{2R_g} + \frac{(R_g + r_e + r_b')^2}{2R_g r_e h_{FE}}. \tag{82}$$

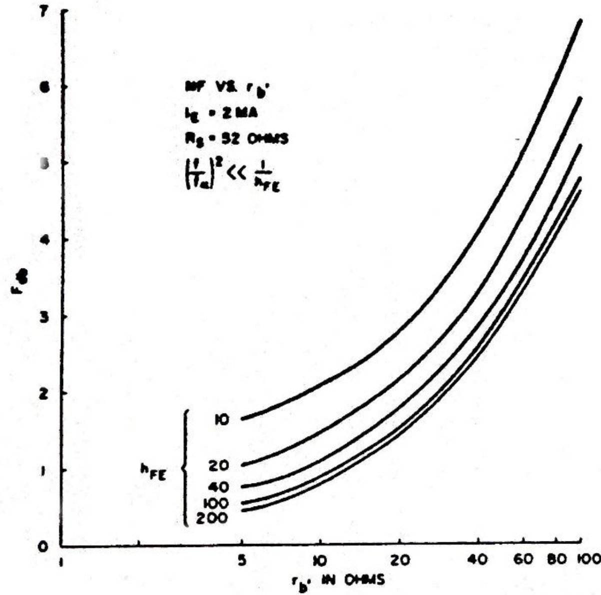

Fig. 17. Graphical solution to r_b' when $R_g = 50\ \Omega$.

A suitable frequency for measuring this noise figure is 1.0 MHz. Since R_g and r_e are known and h_{FE} is easily obtained, (82) can be solved for r_b'. Although the solution is not difficult, it is tedious, and a graphical approach is indicated. Fig. 17 is a graph for one set of test conditions.

Since r_b', or part of it, is frequency dependent, the value obtained by the procedure is the asymptotic low-frequency value. However, the results, when substituted into the noise figure expression (7) and the calculations of Fig. 11, agree very well. This technique is particularly useful in evaluating the contact resistance, since it affects noise figure in the same manner as does r_b'.

E. Measurement of C_{TC}

The total collector capacitance (exclusive of contacts) is obtained most easily by probing the base diffusion before the emitter has been put in. A bridge or direct reading meter can be used for the measurement. Care should be taken to balance the instrument with the probe in position but not quite touching the base area.

The contact capacitance can be obtained by probing the completed chip and subtracting out the device collector capacitance.

Collector capacitance under the emitter (C_{C1} or C_{Ci}) can be obtained for a simple low-frequency transistor by measuring the $r_b'C_C$ time constant and dividing by r_b'. For microwave transistors the time constant is somewhat more complex and should actually be referred to as $h_{12}/j\omega$. Section IV-H gives more detail on h_{12}.

F. Measurement of ρ_{epi}

This is the resistivity of the collector epitaxial region. It is obtained by making a diffusion into the epitaxial layer, either as a special diode or as the base of a transistor. The capacitance is then measured as a function of the applied voltage (i.e., reverse bias) from a fraction of a volt up to breakdown, or to where $\Delta C/\Delta V$ becomes 0. Which occurs first will depend upon ρ, the depth of the diffusion, and the thickness of the epitaxial film. For n-type silicon in the 1-10-$\Omega\cdot$cm range,

$$\rho \cong \frac{1.77(A_{mil^2})^2 \times 10^{-2}}{(V+\phi)C_{pF}^2}\ \Omega\cdot\text{cm}. \tag{83}$$

Note that ϕ, the contact potential or barrier voltage, appears

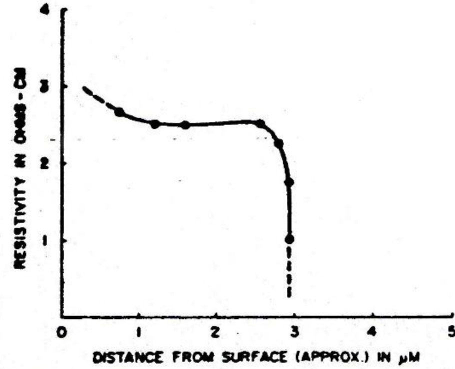

Fig. 18. Plot of ρ versus X_d for an epitaxial film.

in (83). It can be eliminated from the equation by taking the differential and then evaluating the slope of the capacitance versus voltage curve. The differential method is extremely tedious and requires a a computer for accurate evaluation. On the other hand, if ϕ is known with a reasonable degree of accuracy and the epitaxial film is not so thin that it depletes out at a very small voltage, then a value for ϕ can be assumed without impairing the usefulness of this approximation.

From the same measurement the depletion-layer width X_d, can be obtained.

$$X_d = \frac{A_{mil^2} \times 6.7 \times 10^{-2}}{C_{pF}}\ \mu\text{m}. \tag{84}$$

A typical curve of ρ versus X_d is shown in Fig. 18. This is an actual plot made from a transistor base diffusion. Note the very abrupt transition from n to n$^+$. This is characteristic of epitaxial material grown by a low-temperature process. It is obvious that this measurement also yields another important parameter, the thickness of the epitaxial region.

G. Measurement of C_{TE}

The emitter transition capacitance can be obtained from the plot of $1/I_E$ versus $1/f_T$. If the depletion-layer transit time and collector time constant are neglected, then

$$\frac{1}{\omega_T} \cong \frac{kT}{qI_E}\cdot(C_{TE}+C_{TC}+C_X)+\frac{1}{\omega_{Ti}}. \tag{85}$$

The slope of (85) is

$$\frac{d\left(\frac{1}{f_T}\right)}{d\left(\frac{1}{I_E}\right)} = \frac{kT}{q}(C_{TE}+C_{TC}+C_X). \tag{86}$$

Therefore, the slope divided by a constant kT/q is $(C_{TE}+C_{TC}+C_X)$. A typical plot is given in Fig. 19. C_X and C_{TC} are determined from the previous section and must be subtracted from (86) to obtain C_{TE} alone. The extrapolation of the linear portion of the curve through 0 (i.e., $I_E=\infty$) yields ω_{Ti}. The value thus obtained for ω_{Ti} will not be the intrinsic value but will also include the collector depletion-layer transit time, i.e.,

$$\frac{1}{\omega_{Ti\,meas}} = \frac{1}{\omega_{Ti}} + \frac{1}{\omega_d}. \tag{87}$$

The correction can easily be made remembering that

$$\frac{1}{\omega_d} = \frac{X_d}{2V_{sL}} \tag{43}$$

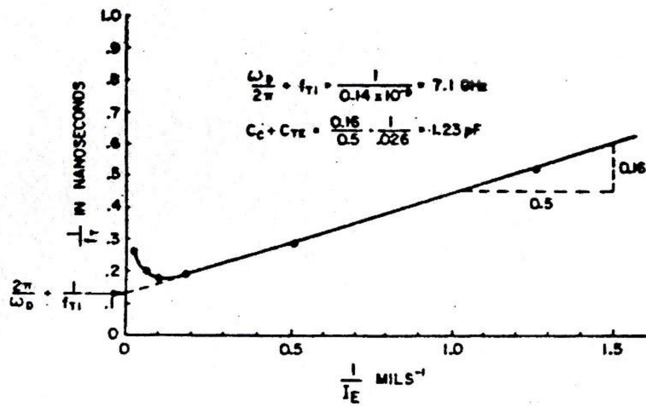
Fig. 19. $1/I_E$ versus $1/f_T$ plot.

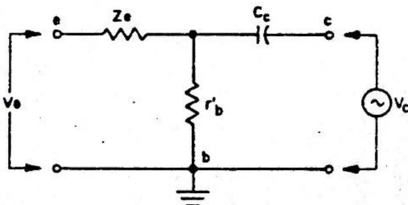
Fig. 20. Equivalent circuit for deriving h_{rb} and $r_b'C_C$.

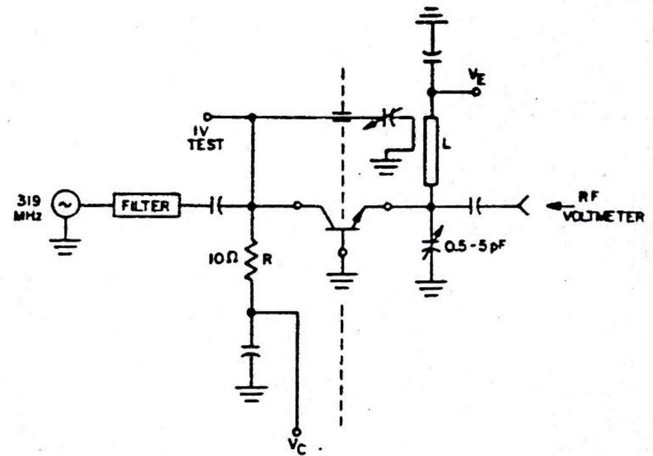
Fig. 21. $r_b'C_C$ test fixture.

and

$$X_d = \left[\frac{2\varepsilon\varepsilon_0(V + \phi)}{qN}\right]^{\frac{1}{2}}. \tag{88}$$

These can be combined with (68) to yield for n-type silicon,

$$\frac{1}{\omega_d} = 3 \times 10^{12}[\rho(V + \phi)]^{\frac{1}{2}}. \tag{89}$$

H. Measurement of $r_b'C_C$

This parameter is related to h_{12b} such that

$$|h_{12b}| = \omega r_b' C_C \tag{90}$$

where h_{12b} is the common base reverse voltage transfer ratio. It is derived from the simplified model given in Fig. 20, where it is obvious that

$$h_{12b} \doteq \frac{V_e}{V_C} = \frac{r_b'}{r_b' + \dfrac{1}{j\omega C_C}}. \tag{91}$$

If ω is selected properly,

$$1/\omega C_C >> r_b',$$

and

$$|h_{12b}| \cong \omega r_b' C_C. \tag{92}$$

The model given above is much too simple for a microwave transistor. However, the total $r_b'C_C$ product that will be obtained by this measurement is still of use. Base on Fig. 11 a more exact expression for h_{12} is

$$h_{12} \cong j\omega(r_{b_1}'C_{C_1} + r_{b_2}'C_{C_2} + r_{b_3}'C_{C_3} + R_C'(C_{C_{metal}}) + r_{b_2}'C_{C_1} + r_{b_3}'C_{C_1} + r_{b_3}'C_{C_2}). \tag{93}$$

To dissect (93) into its various components is a tedious job requiring many measurements. The contact resistance is best obtained from a test pattern on the chip and the other portions of C_C by scaling from known dimensions.

The measurement of h_{12b} is simple in theory but difficult to implement due to the very high ratio of V_c/V_e for a good microwave transistor. For example, if r_b' equals 20 Ω, C_C equals 0.02 pF, and f equals 320 MHz, then

$$|h_{12b}| \cong 8 \times 10^{-4}.$$

A test signal of 1 V for V_c is near the maximum allowable while still maintaining small-signal conditions; this makes V_e for the above calculation equal to approximately 0.8 mV. Standard RF voltmeters usually have a maximum sensitivity of 1.0 mV full scale, and 0.8 mV is read on the meter scale with the poorest accuracy. This indicates that a higher test frequency is desirable, but with the attendant problems in isolation.

An $r_b'C_C$ test fixture requires some form of neutralization to cancel out the residual capacity of the fixture itself and that of the transistor package. Fig. 21 shows one form of such a test circuit. The circuit also includes a filter to attenuate the harmonics of the test signal. An output tank circuit allows tuning of the probe and other distributed capacity. The test frequency 319 MHz, was selected so that with $V_c = 1$ V, r_bC_C in picoseconds is $V_e/2$. In order to maintain the high isolation required, this fixture should be built in the form of a box with milled cavities.

V. Conclusion

The theory of microwave transistors and their limitations has been well established, and performance can be predicted with reasonable accuracy. New technologies developed in the past five years have made it possible to approach frequency limits more closely than was first thought possible. The present era is one of new fabrication technologies rather than breakthroughs in theory. Radiation as an adjunct or replacement for diffusion, electron beam masking, etc., is being used to make better transistors, but the materials limitations still exist and are not likely to change. In the next year or so, small-signal transistors will become useful in the X band and power devices in the C band. Power transistors will not replace tubes where the very high peak powers are required. However, in phased array systems where modest average powers are needed, the transistor will eventually predominate. At the lower end of the microwave region near 1 GHz, small-signal transistors will continue to replace paramps as the 1-dB-maximum noise figure limit moves into the 1–2-GHz band.

Nomenclature

Symbol	Definition
α	Common-base current gain.
α_0	Common-base current gain at low frequencies.
α_i	Intrinsic alpha determined by base transport only.
β^*	Base transport factor: the ratio of minority carriers injected from the emitter into the base to the number arriving at the base edge of the collector–base depletion layer.
β_0^*	Low-frequency value of β^*.
β_m	Collector–depletion-layer transport factor: the ratio of carriers leaving the collector–base depletion layer to those entering it from the base.
γ	Emitter injection efficiency: the ratio of the minority carrier current injected into the base from the emitter to the total emitter current.
γ_{hf}	High-frequency value of γ.
γ_0	Low-frequency value of γ.
Δf	Bandwidth (Hz).
ε	Relative dielectric constant.
ε_0	Permittivity of free space.
η	Drift field factor.
θ	Thermal resistance (°C/W).
μ	Mobility.
μm	Distance in microns.
π	The constant, 3.1416 ···
ρ	Resistivity ($\Omega \cdot$ cm).
τ	A time constant.
τ_B	Minority carrier lifetime in base region.
τ_b	Base transit time.
τ_c	Collector capacitance–resistance charging time.
τ_d	Collector depletion-layer time constant.
τ_e	Emitter capacitance–resistance changing time.
τ_{ec}	Transit time for carriers from emitter to collector.
τ_m	Collector depletion-layer transit time.
ϕ	Contact potential of a junction.
ω	Radian frequency, $2\pi f$.
ω_α, ω_β, ω_0, ω_T, ω_{Ti}	See f_α, f_β, etc.
A	Area in general.
A_{mil^2}	Area (mil²).
A_c	Collector area.
A_e	Emitter area.
C_C	Capacitance of collector–base junction.
C_E	Capacitance of emitter–base junction.
C_{DC}	Diffusion capacitance of collector–base junction.
C_{DE}	Diffusion capacitance of emitter–base junction.
C_{TC}	Transition capacitance of collector–base junction.
C_{TE}	Transition capacitance of emitter–base junction.
C_{CI}	Collector capacitance (inner) under emitter.
C_{CO}	Collector capacitance (outer) outside emitter.
C_{C1}, C_{C2}, C_{C3}	Components of collector capacity.
D	Diffusion constant, for minority carriers.
E	Electric field (V/m).
e_{nb}	Thermal noise voltage due to base resistance.
$\overline{e_{nb}^2}$	Mean-square value of base thermal noise voltage.
F	Noise factor (figure).
F_p	Plateau noise figure: noise figure of a transistor in middle-frequency range, where $dF/df = 0$.
f	Frequency.
f_α	Frequency where $\lvert\alpha\rvert$ has dropped to $\sqrt{2}/2$.
f_{hfe}	Frequency where $\lvert h_{fe}\rvert$ has dropped to $(\sqrt{2}/2)h_{fe0}$.
f_β	Frequency where $\lvert\beta^*\rvert$ has dropped to $(\sqrt{2}/2)\beta_0^*$.
f_c	Upper noise corner frequency, where $F = F_p + 3$ dB.
f_0	A characteristic frequency [see (28)], $= 1/2\pi(W^2/2D)$.
f_T	Frequency where the extrapolated $\lvert h_{fe}\rvert$ goes to unity.
f_{Ti}	Intrinsic value of f_t as determined by base transit time only.
f_{max}	Maximum frequency of oscillation; the highest frequency at which a device will oscillate in a lossless circuit, or the frequency where the unilateral gain is unity.
G	Gain.
G_0	Low-frequency gain.
G_{max}	Maximum available gain (sometimes called MAG): gain of an unconditionally stable device when input and output are simultaneously conjugately matched.
h_{fe}	Common-emitter current gain.
h_{FE}	Dc common-emitter current gain.
h_{fe0}	Low-frequency common-emitter current gain.
I_c	Dc collector current.
I_{co}	Collector cutoff (a leakage) current.
I_E	Dc emitter current.
i_{ne}	Emitter shot noise current.
$\overline{i_{ne}^2}$	Emitter shot noise current, mean-square value.
i_{nc}	Collector shot noise current.
$\overline{i_{nc}^2}$	Collector shot noise current, mean-square value.
i_e	Signal current flowing into active part of emitter admittance.
i_{et}	Total signal current flowing into emitter terminal.
K	An arbitrary constant.
k	Boltzmann's constant, $= 1.38 \times 10^{-23}$ J/°K.
L	Diffusion length; average distance carriers will diffuse before recombining.
L_b	Base lead inductance.
L_e	Emitter lead inductance.
l	Length.
M	Noise measure.
N	Impurity concentration (atoms/cm³).
N_{BC}	Impurity concentration in base at collector edge.
N_{BE}	Impurity concentration in base at emitter edge.
N_C	Impurity concentration in collector adjacent to base.
P_D	Power dissipated.
q	Electronic charge, $= 1.6 \times 10^{-19}$ C.
R_{BB}	Base sheet resistance.
R_{EE}	Emitter sheet resistance.
R_g	Source resistance, for noise measurement.
r_c'	High-frequency collector series resistance.
r_b'	Base spreading resistance.
r_{b1}', r_{b2}', r_{b3}'	Components of r_b'.
r_e	Emitter resistance, $= kT/qI_E$.
S	Stripe dimension, in general.
S_1, S_2, S_3	Refer to Fig. 11.
t	Time.
T	Temperature (°K).
T_j	Transistor junction temperature.
T_s	Transistor heat sink temperature.
U	Unilateral gain; the gain of a device with a lossless unilateralizing network and both ports conjugately matched.

V_{SL} Scattering limited velocity of carriers.
W Base width.
W_1, W_2, W_3 Widths in transistor geometry (refer to Fig. 11).
X_d Depletion-layer width.
X_{dc} Collector–base junction depletion-layer width.
X_{de} Emitter–base junction depletion-layer width.
Z_{in} Input impedance of a transistor.
Z_{out} Output impedance of a transistor.
Z_c Collector impedance.
Z_e Emitter impedance.

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