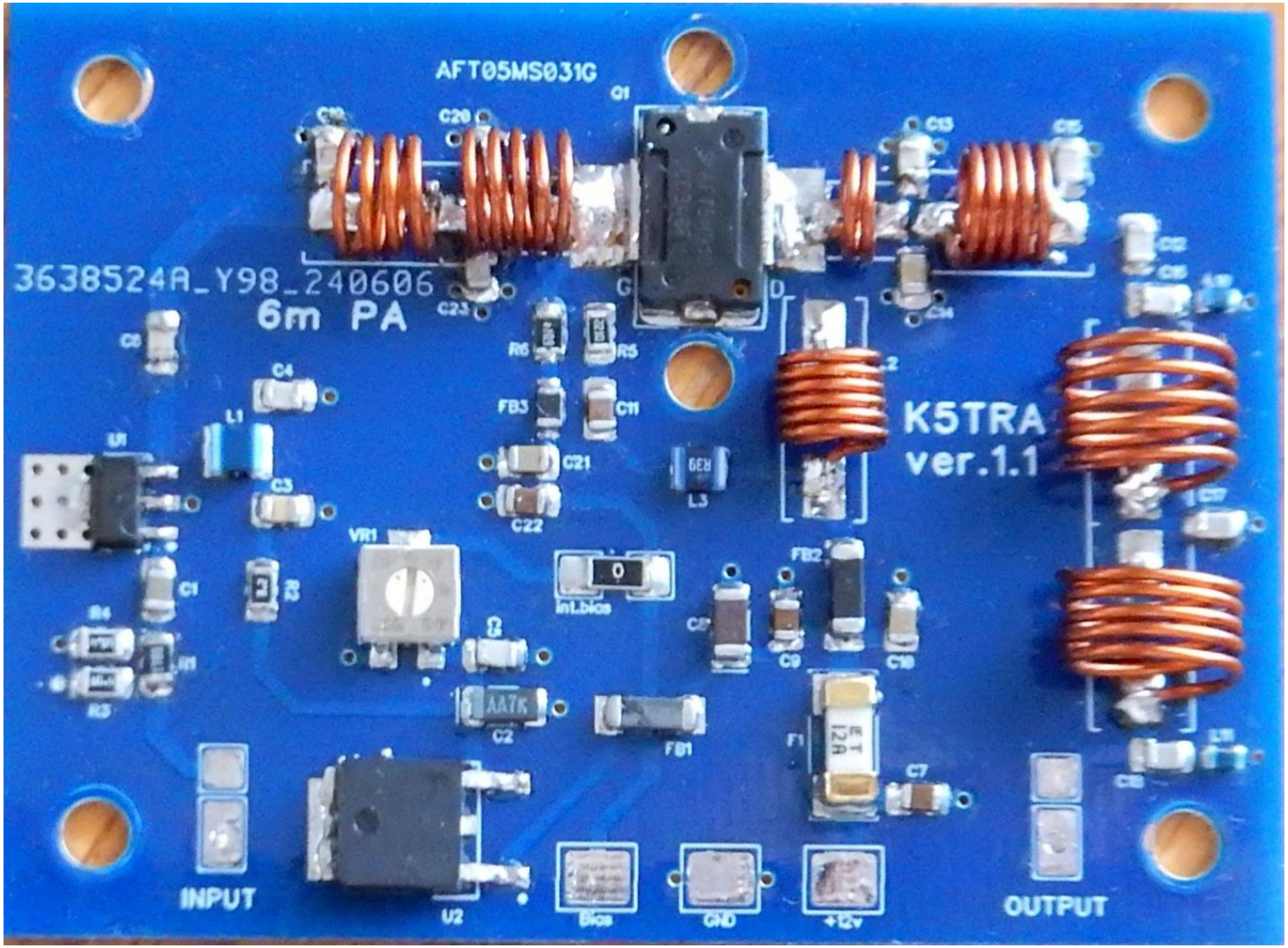
6m LDMOS FET PA

20W , + 48 dB gain

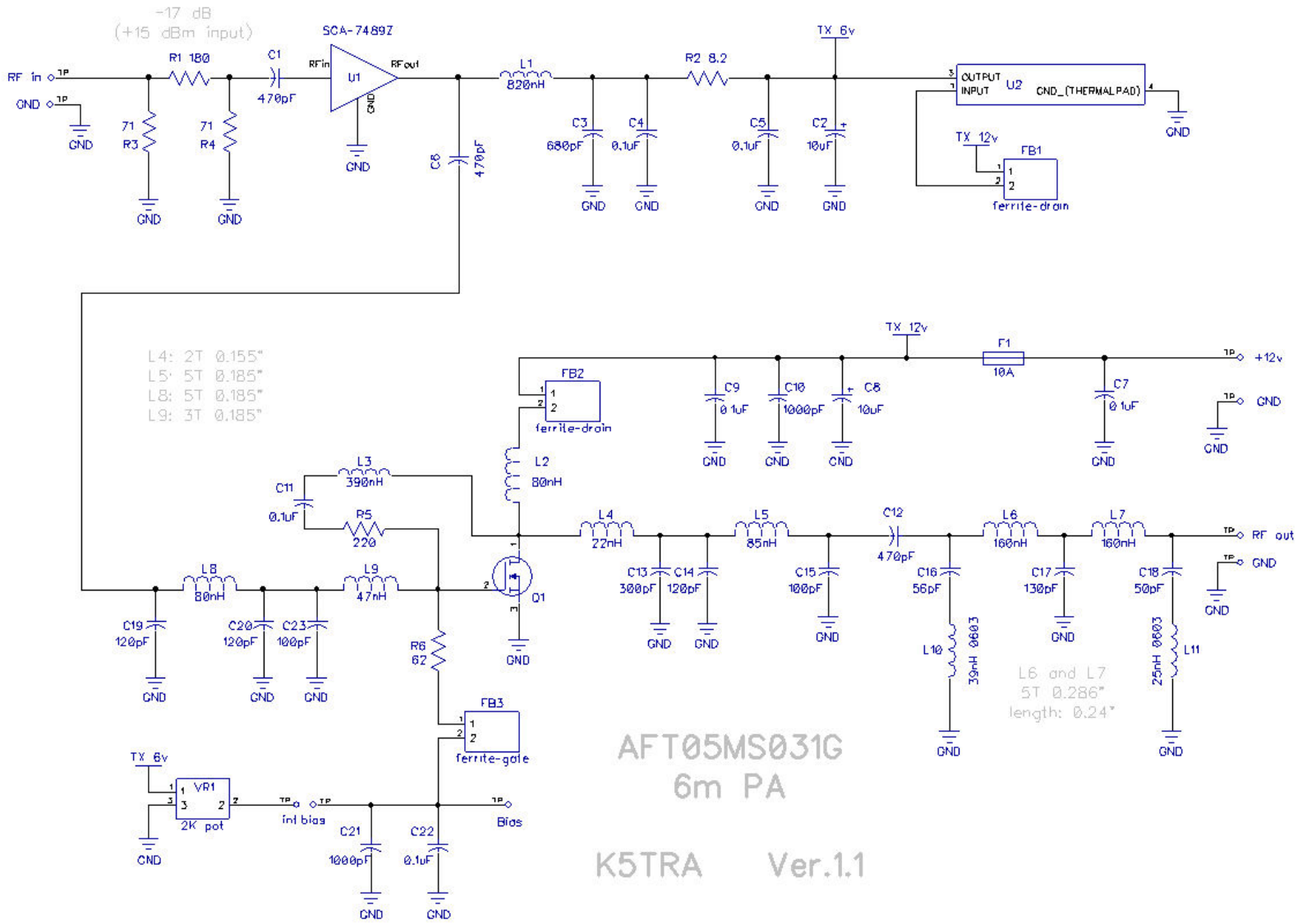
OVERVIEW

- NXP LDMOS power FET
  - AFT05MS031G
  - 500 MHz capable
  - 30 W capable
  - 29 dB gain (with feedback) at 50 MHz
- SGA-7389 driver
  - 2 GHz capable
  - 22 dBm capable
  - 22 dB gain
- Input attenuator to set gain (max gain: +48 dB)
- Output low pass filter
- Internal and external bias options
- 2.5” x 1.85” (0.04” FR4) board

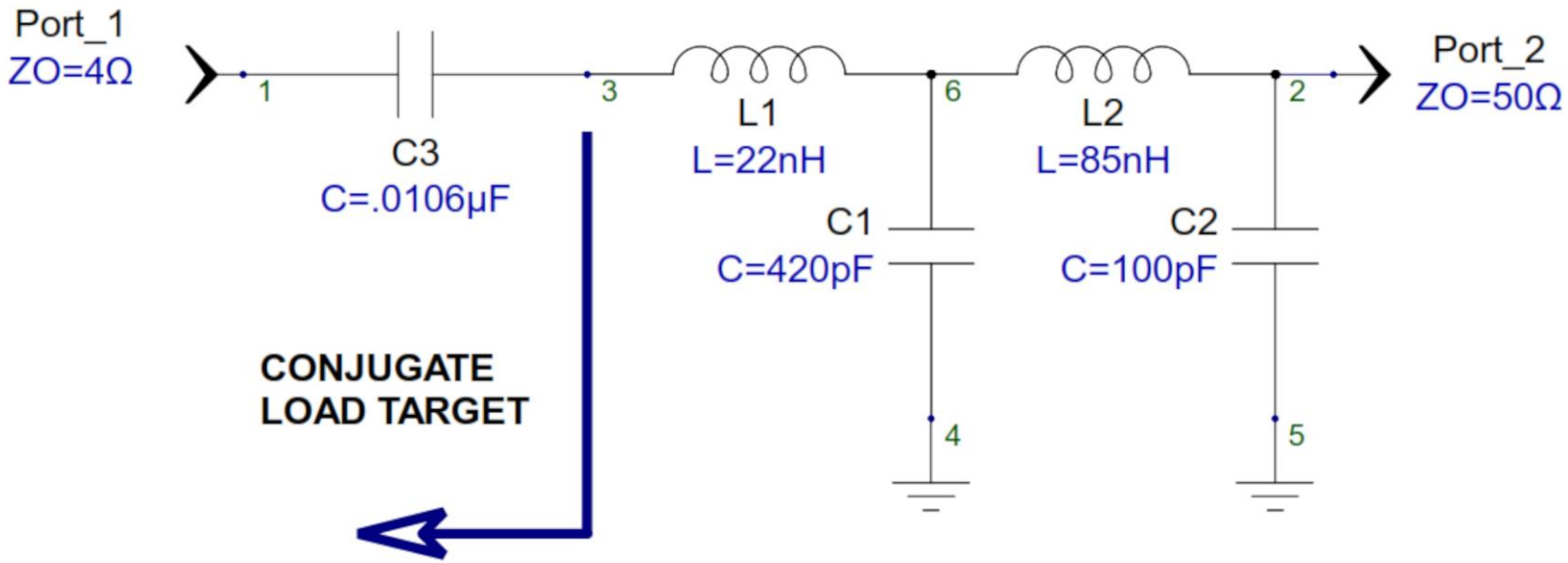
20W POWER AMPLIFIER



PA SCHEMATIC



OUTPUT MATCH DESIGN

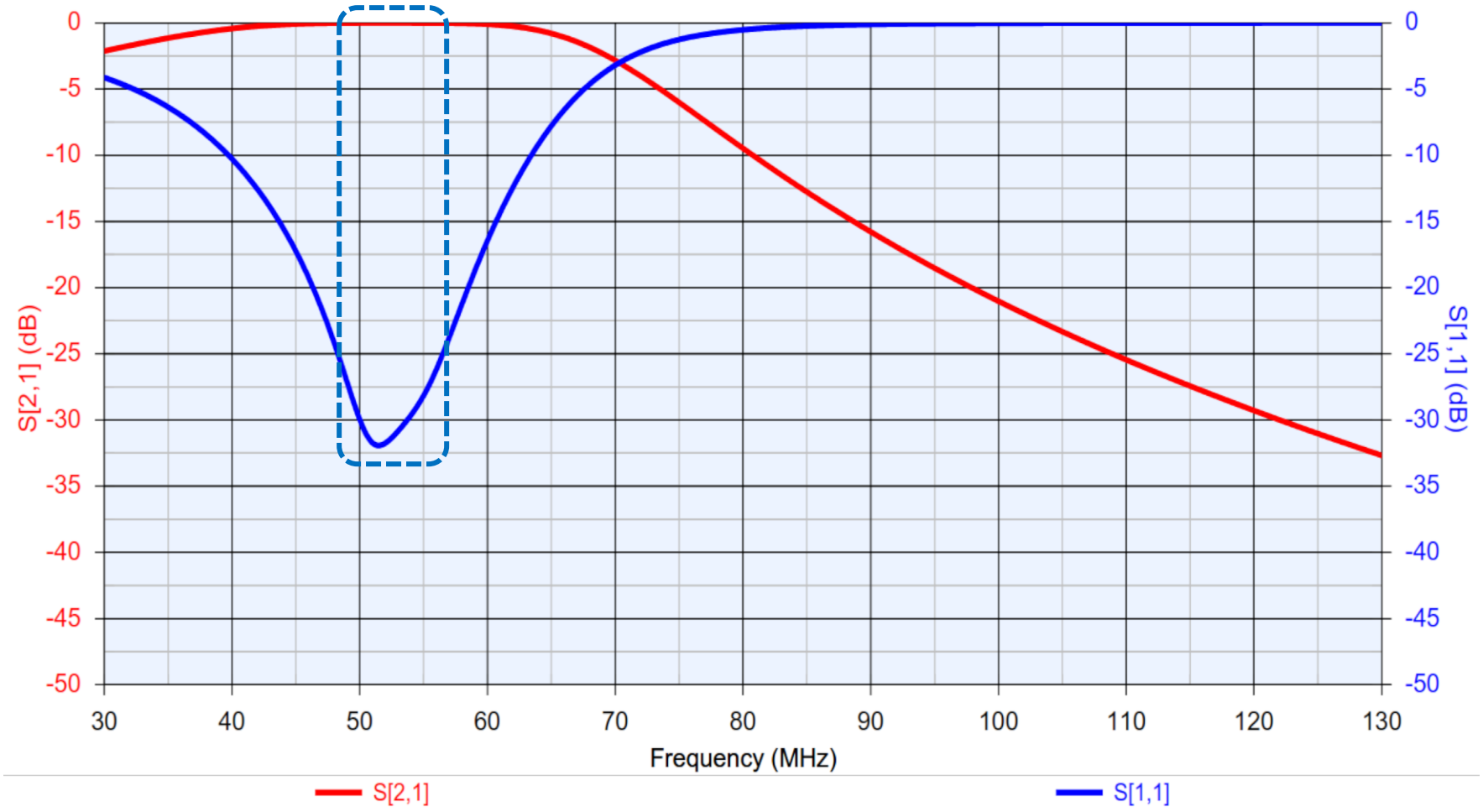


$$R_L = \frac{(Vdd\ - 1)^2}{2\ Pout} = \frac{12.6^2}{40} = 4\ \Omega$$

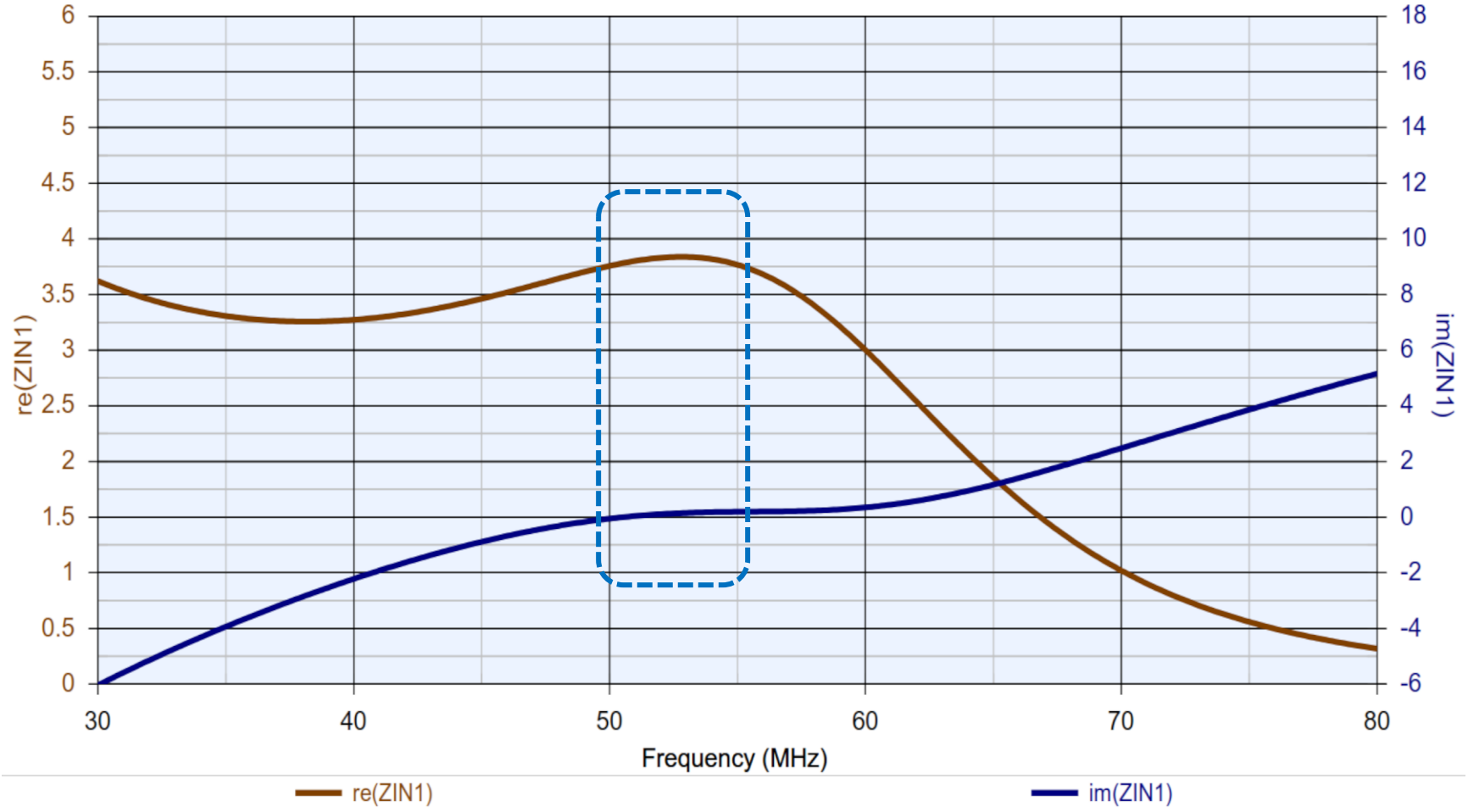
$$C_{OUT} = 50\ pF$$

SERIES EQUIV: $4\ \Omega + 0.01\ uF$

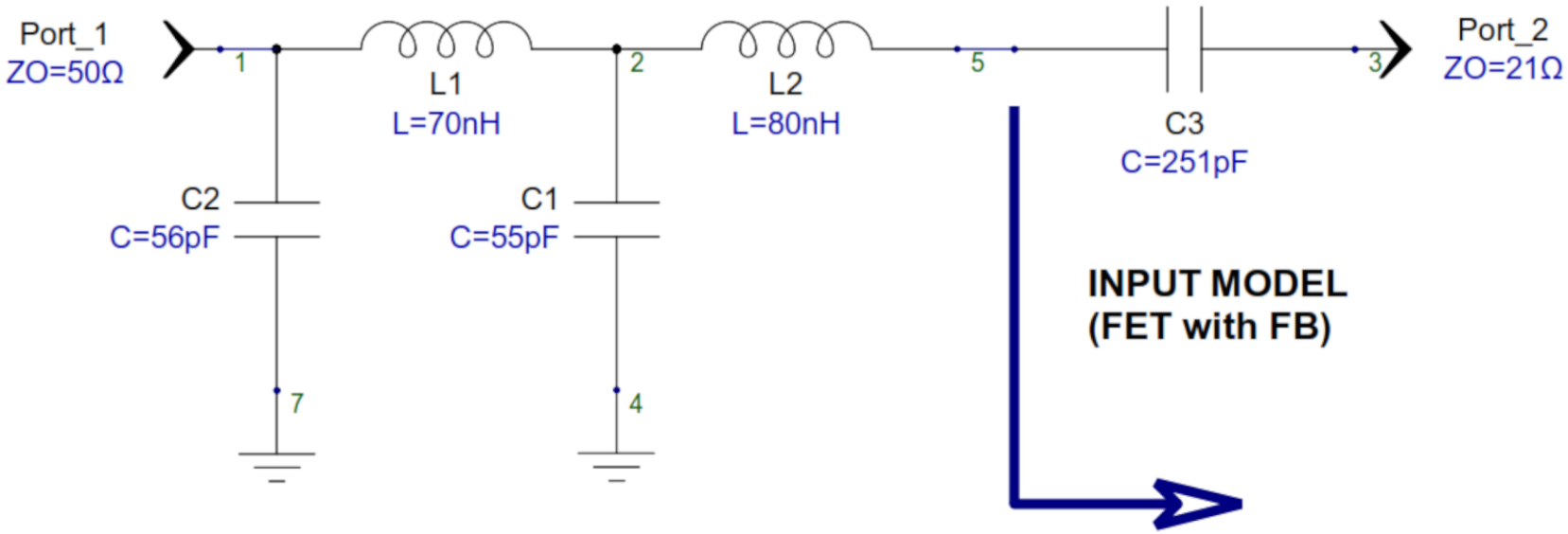
DRAIN (OUTPUT) MATCH



LOAD IMPEDANCE PERFORMANCE

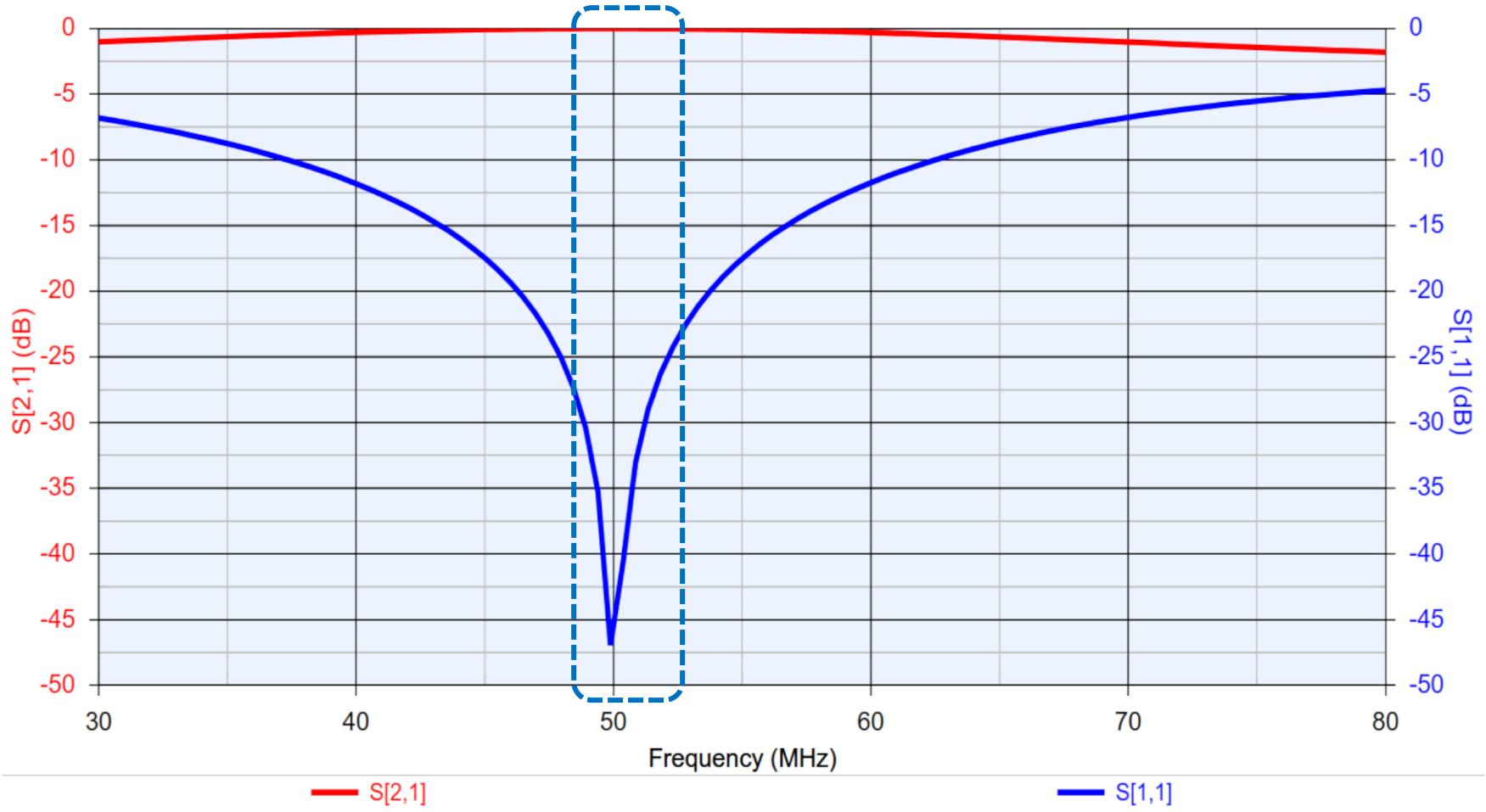


INPUT MATCH DESIGN

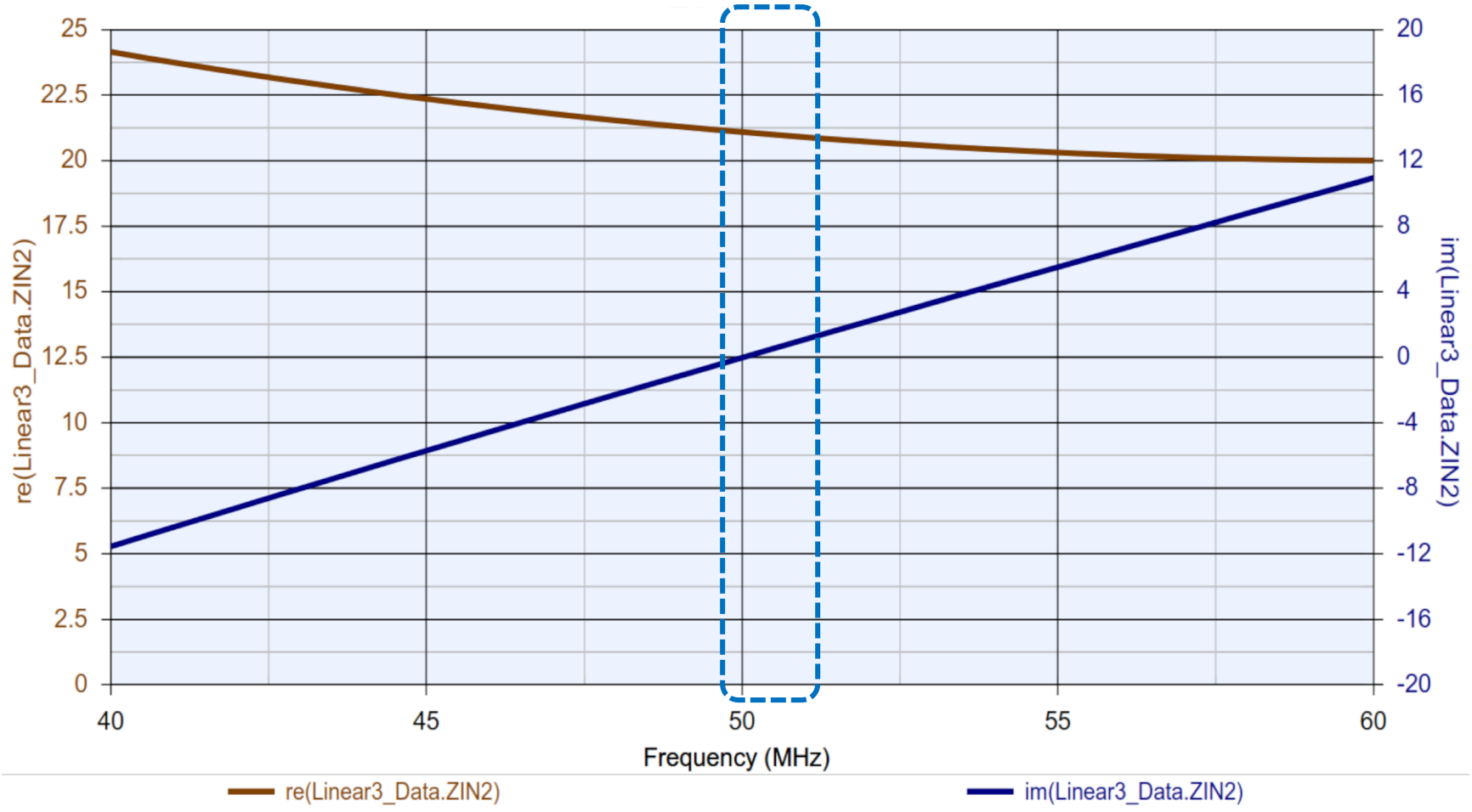


- 21 Ω + 251 pF is FET input (with FB)
- Measured through single section LC prematch
- De-embedded to gate
- Represented in series equivalent impedance form

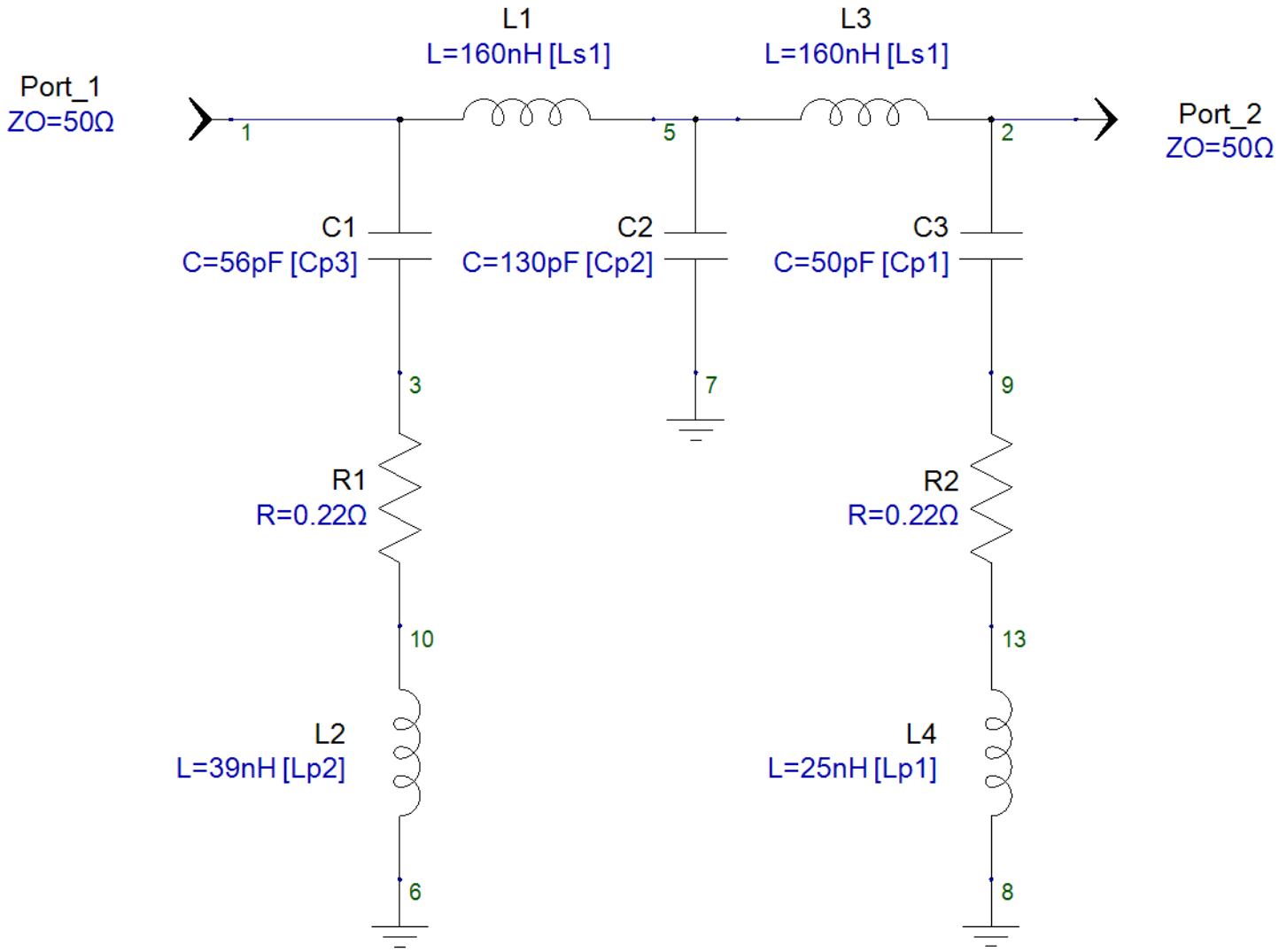
GATE (INPUT) MATCH



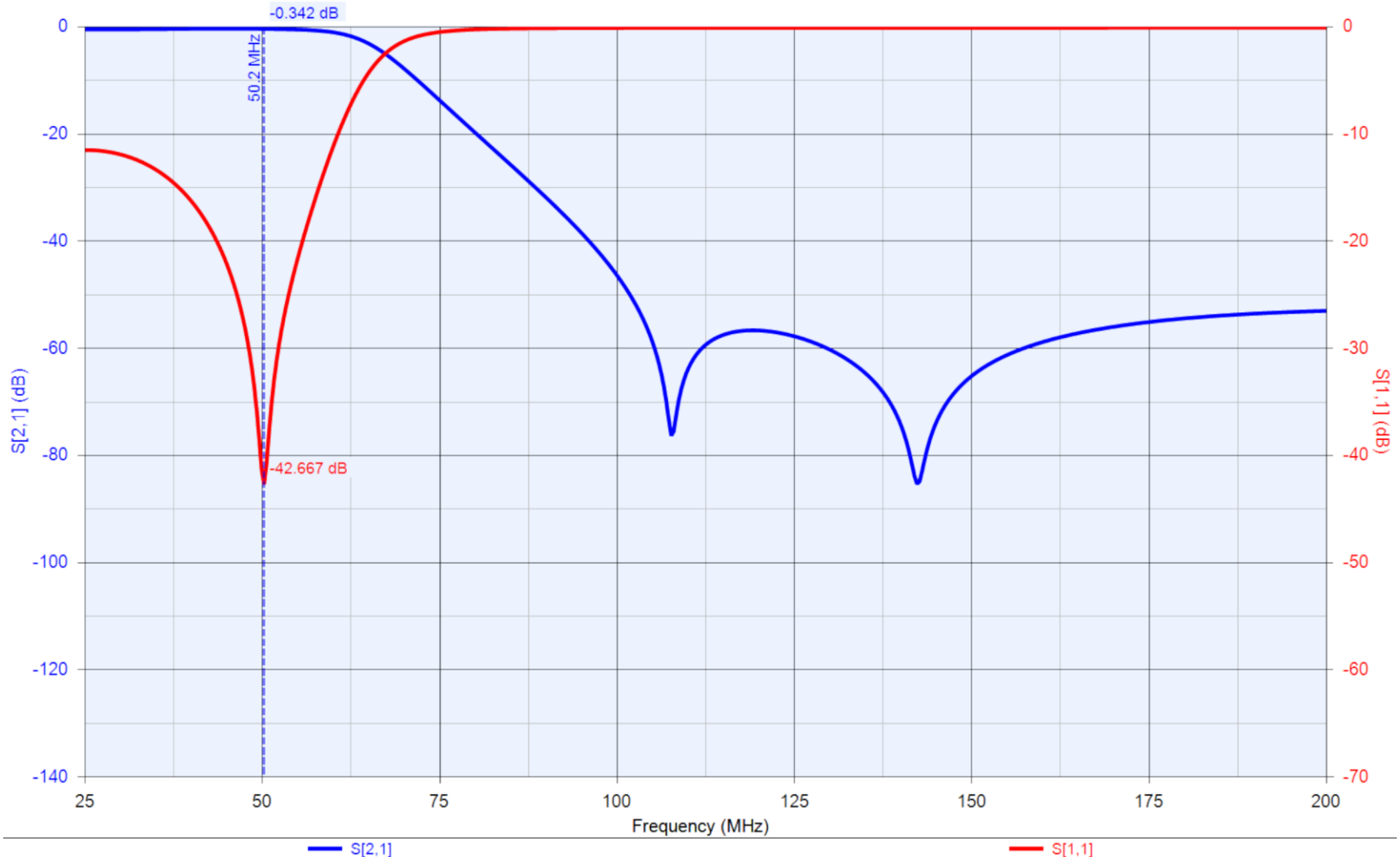
SOURCE IMPEDANCE PERFORMANCE



PA LPF


L1
L=160nH [Ls1]
L3
L=160nH [Ls1]
Port_1
ZO=50Ω
Port_2
ZO=50Ω
1
5
2
C1
C=56pF [Cp3]
C2
C=130pF [Cp2]
C3
C=50pF [Cp1]
3
7
9
R1
R=0.22Ω
R2
R=0.22Ω
10
13
L2
L=39nH [Lp2]
L4
L=25nH [Lp1]
6
8

LPF RESPONSE



SUMMARY

- New PA with NXP AFT05MS031G LDMOS power FET instead Mitsubishi module
- FET is 30W capable with loading set for 20W output
- Internal filtering: harmonics < -80 dBc
- Max gain: +48 dB with input pad set to 0 dB
- Negative FB on final provides very stable operation
- Internal or external bias (jumper) options
- 2.5” x 1.85” (0.04” FR4) board