Pushpull Power Amplifiers for Handsets

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Technology Development

***Abstract* — Design of pushpull power amplifiers for handset applications is presented. Development of balanced transformers and baluns is detailed. IC realization techniques, such as interleaving of output transistor cells, are also presented. Examples are presented in cellular band and PCS in addition to a wideband PA that spans more than an octave (0.8 GHz to 2 GHz).**

***Index Terms* — Pushpull, baluns, power amplifiers.**

I. Introduction

Handset power amplifier performance targets continue to become more challenging. Linearity and power efficiency performance that was competitive two years ago will not be in the future. The challenge is further compounded by system demands for more bandwidth and the desire to have power amplifiers support multiple (all) operating modulation modes. Both multiple mode and multiple band interests are driven by cost reduction considerations.

The most significant design aspect leading to handset power amplifier performance limitations is the low load impedance required to support the output power requirement from a low voltage DC supply. As operating voltage is lowered, several effects conspire to reduce power efficiency. First, knee voltage drop in the transistor, at high current, represents a larger fraction of the available peak voltage (set by the DC supply). For a given power output, as the peak voltage is reduced, the corresponding current must increase. This lowering of load impedance leads to the second contribution to performance reduction. The output matching network must transform the external 50Ω load to the low impedance load at the transistor. Loss increases as transformation ratio is increased. Bandwidth is almost always compromised as load impedances are lowered.

Several general principals are suggested: 1) raise the operating voltage whenever you can, and 2) reduce the impedance transformation ratio in the matching network whenever you can. The supply voltage to the PA could be raised by a DC-DC boost converter. However, this isn't always possible. A reduction in transformation ratio is possible without changing the DC supply voltage. By departing from conventional "all cells in parallel" single-ended thinking, we can gain a four-fold advantage in transformation ratio reduction from differential (also called pushpull) operation. An example of this type of PA can be seen in Figs. 1 and 2. The chip photo in Fig.1 shows a two stage PA with integrated balun input. The laminate module photo in Fig.2 provides a low loss balun to impedance match the PA die.

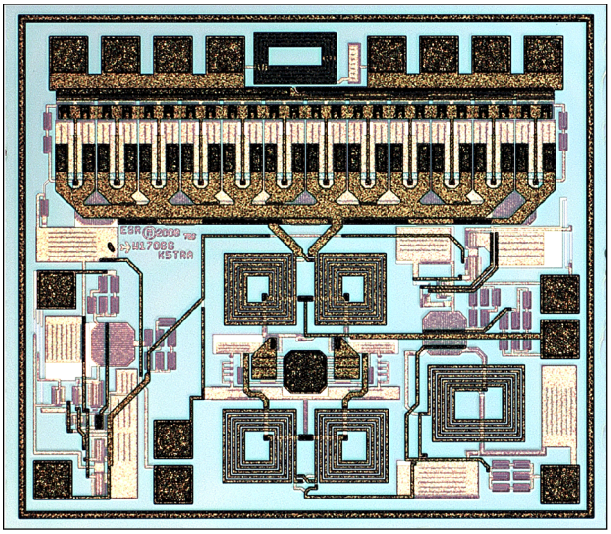

Fig.1. Cellular pushpull PA die

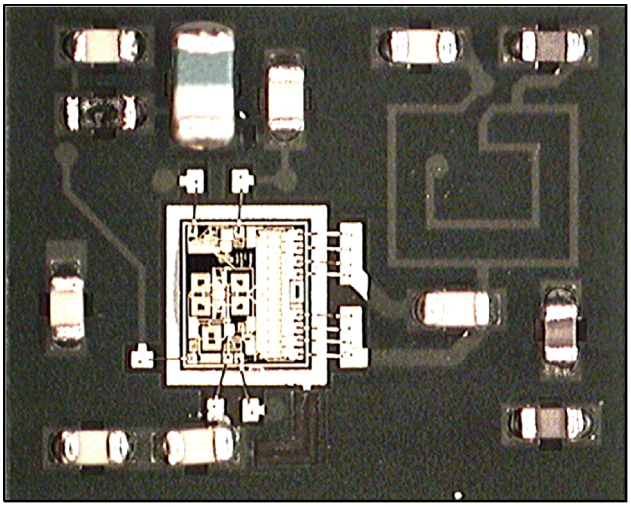

Fig.2. Cellular pushpull PA module

II. Advantages of Differential Operation

If one considers all transistor segments operating in phase as single-ended, then the conceptual partition of those cells into two clusters can be useful in view of the relationship between single-ended and differential (also called pushpull). Proper load sharing would suggest both clusters see the same load, 2x the external load. The RF current flowing through each cluster is half of the total and the same RF voltage is seen by all cells in parallel. As an alternative, if we operate the same two clusters of cells out of phase by 180 degrees, then each must see the same optimum load. The RF voltages and currents are; however, 180 degrees out of phase. The total load voltage is twice the voltage across an individual cluster, while the total current is the same. In other words, the external differential load is twice that of one cluster. So, the differential load is four times the single-ended load for the same number of cells, supply voltage, and power output! This significant advantage is illustrated in Fig.3.

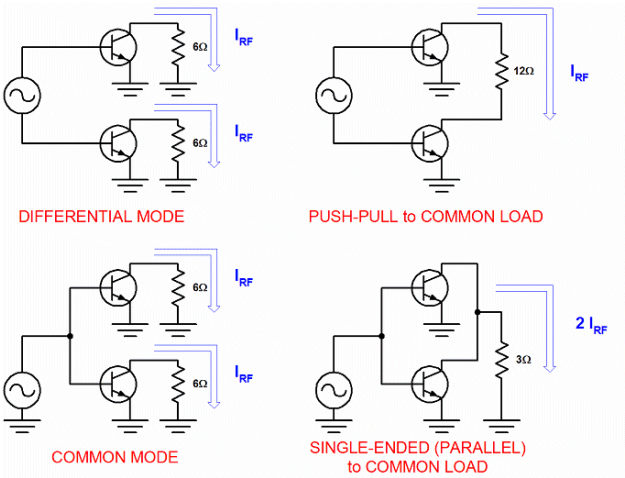

Fig.3. Relationship between single-ended loading and pushpull loading.

At this point, in order to avoid confusion, it is important to recognize that several terms are synonymous. Differential mode, odd mode or pushpull operation all have the same meaning in pushpull amplifiers. Similarly, common mode, even mode, and single-ended operation may be interchanged.

Both sides of pushpull amplifiers are usually biased from a common bias source. So, from a DC perspective, operation is in parallel (common mode). When distortion produces harmonics, odd order Fourier terms maintain differential mode symmetry, while even order Fourier terms appear in the common mode. This additional degree of freedom provided within pushpull amplifiers can be used to considerable advantage. While maintaining balance in the differential mode, a natural suppression of second harmonic levels from the output is present. It is important to point out that this applies to second harmonic levels *generated* in the pushpull PA stage. Any drive from previous stages at second harmonic frequencies will, of course, be amplified like any other odd mode input signal.

Some of the advantages pushpull PAs offer over single-ended PAs are:

1) Four times greater load impedance for given power and supply voltage,
2) Separation of even and odd harmonic frequency terms,
3) Elimination of high current in a common mode bypass path,
4) Significant reduction in RF ground currents,
5) Means to provide 2nd harmonic short over a broad band for linear amplifiers,
6) Reduction in 2nd harmonic levels due to common mode isolation,
7) Isolation of RF from bias circuit due to common mode isolation,
8) BW performance more readily achieved due to higher impedance operation.

III. Challenges

One well might ask, if pushpull has so many advantages, why isn't it in widespread use in handset applications? It is very much in widespread use at lower frequencies (3 MHz through 450 MHz). It is also used in some high power pulsed avionics and in some cellular base station PAs. In all cases, the enabling circuit element is a low loss balun in the output circuit. For handset applications, this must also be small enough for module integration. Loss has been the roadblock for acceptably small baluns. Lack of such an element has been the primary impediment to pushpull PA development for handset applications. Low frequency balun and balanced transformer implementations are not well suited for use in handsets. They are usually formed from twisted wire pairs or small coax lengths and often ferrite loaded. A direct use of these techniques is too large and limited in upper frequency. Small surface mount baluns, such as those sold by mini-circuits are

too lossy for competitive handset power amplifiers. Losses should be under 0.5 dB and the size of the overall output match should at least be competitive with current single-ended matches.

Input baluns should be integrated into the PA IC. Similarly, the interstage match in the IC should have an integrated balanced transformer.

Since balanced transformers and baluns are the gating elements in successful pushpull power amplifiers for handsets, they will be discussed next.

IV. Balanced Transformers and Baluns

Transformers can be realized in classic form where the only coupling mechanism is magnetic flux, or as composites of coupled transmission line unit blocks. Examples of the transmission line transformers are single-ended Ruthroff [1] and balanced Guanella [2] transformers [3,4].

Classic flux coupled transformers are comprised of separate tightly coupled inductors. For low loss and wide bandwidth, coupling near unity (k>0.9) is desired. Distributed capacitance causes self resonance and kills high frequency performance.

Transmission line transformers are comprised of segments of coupled transmission lines. Unlike the classic flux (only) coupled transformers, the finite impedance of the transmission line provides a natural mechanism for dealing with non zero, real world, distributed capacitance. Losses are also lower, for a given media, due to energy coupling by both flux coupling and by a conducted path. For both of these reasons, one can confidently say that transmission line transformers will always outperform flux (only) coupled transformers in the same media.

Before we jump into a discussion of balanced transformers (sometimes called balbal structures) and balanced to unbalanced transformers (also called balun structures), let's look at single-ended cases. Fig.4 illustrates a single-ended transformer from both cases. Conventional transformers provide impedance transformation proportional to the square of the turns ratio. Voltage ratios follow the turns ratio and current ratios are inversely proportional to the turns ratio. Transmission line transformers are comprised of unit elements that are often represented as 1:1 transformers. Flux coupling requires equal and opposite directed currents in these unit element lines. By inspection, we can see that the Ruthroff transformer in Fig.4 provides double the current at the right port, with half the voltage

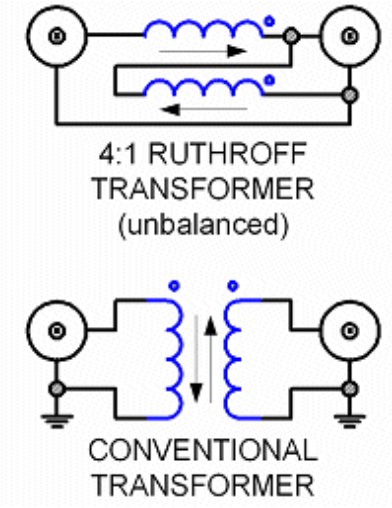

Fig.4 Single-ended transformers: transmission line type (4:1), and conventional flux coupled.

compared to the left port. This is an example of a single-ended 4:1 transmission line transformer.

If we wish to make a balanced to unbalanced transformer (also called a balun), we could simply 'float' the grounded connection on one side of the conventional transformer shown in Fig.4. Better yet, we could ground a center tap on the balanced side (to better force the balance). This can be seen in Fig.5.

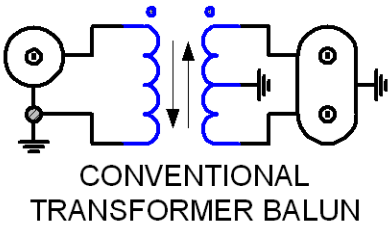

Fig.5 Conventional balanced to unbalanced transformer (BALUN).

Since a performance advantage can be obtained from transmission line related transformer structures, the obvious question is "How can one make transmission line related baluns and balanced transformers?". Consider the two cases illustrated in Fig.6. Both structures are comprised of coupled line unit elements. Allowed currents due to magnetic coupling are shown.

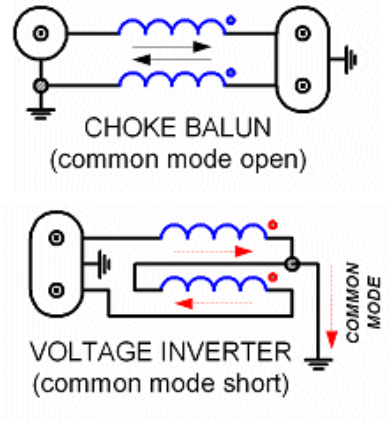

Fig.6 Transmission line balun elements.

The "choke balun" structure behaves as a transmission line in the odd mode (between the conductors) to provide low loss energy flow between the ports. This is always true when the currents are directed equal and opposite, as sketched. Note that any attempt to launch in-phase common mode current into the balance port side is met with a high impedance inductive termination. Ideally, at unity coupling, the common mode impedance becomes infinity. The "choke balun" element provides current balance. Only balanced currents are allowed to flow.

The "voltage inverter" can be thought of as a center taped auto-transformer. Allowed currents are shown in red. Note that these currents are associated with common mode currents. This element provides a short circuit for available common mode current. Ideally, differential mode voltage has no interaction with this element. The common mode short behavior prevents any voltage imbalance when the voltage inverter is placed across the balanced port.

By using a combination of choke balun and voltage inverter elements, a very good broadband low loss 1:1 balun can be formed. Such a structure will be discussed in more detail later.

V. Frequency Compensation of Coupled Lines

Performance of transmission line unit structures can be extended by capacitively compensating non-ideal coupling [5]. To explore this, consider the choke balun shown in Fig.7.

The unit coupled element is best thought of as a pair of coupled transmission lines. The odd mode impedance forms the basis for propagation in the transmission line mode between the conductors. For asymmetric lines [6] this is the π mode.

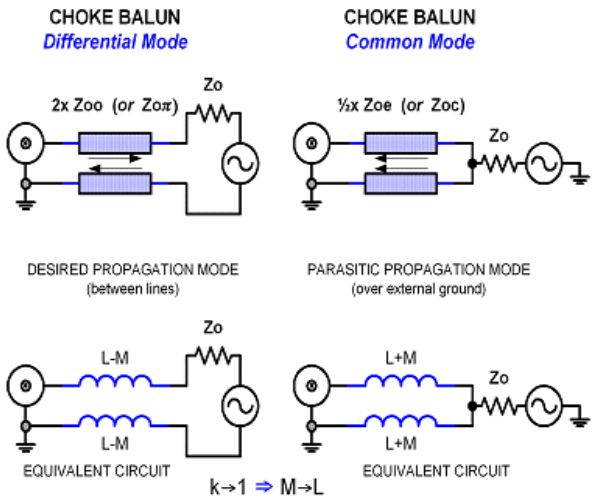

Fig.7 Non-Ideal coupling in choke balun

$$k = \frac{Zoe - Zoo}{Zoe + Zoo}$$

The even mode impedance is a parasitic mode due to an external ground. The higher the ratio between even mode and odd mode impedance, the greater the coupling coefficient. The coupling limit for very high Zoe is unity. This view is useful for optimizing line structures and media choices. For compensation, it is useful to consider the inductive equivalent circuits in Fig.7. In the desired propagation mode, the differential mode inductance, 2(L-M), is to some extent naturally compensated by the odd mode distributed capacitance in that transmission line mode. This is the capacitance associated with 2·Zoo. The even (parasitic) mode causes low frequency performance degradation that requires compensation. To see this, consider the common mode equivalent circuit in Fig.7. Clearly, the common mode balance performance at DC is not good. Rather than an open circuit (high Z inductive), a shunt inductor (L+M) causes a short circuit to ground. A choke balun should deliver power to the balanced port regardless of it's balance condition. For example, if one of the balanced terminals or the other was grounded, power flow should not be perturbed. With this ideal performance in mind, consider Fig.8. We have two cases to consider. The first case is simply a transmission line from input to output. The second case is clearly more troublesome, because there is no conducted path between input and output

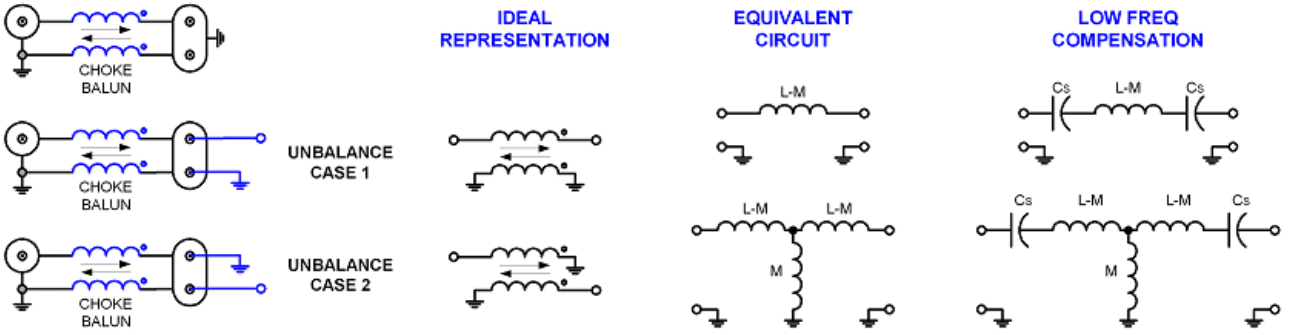

Fig.8 Low frequency compensation

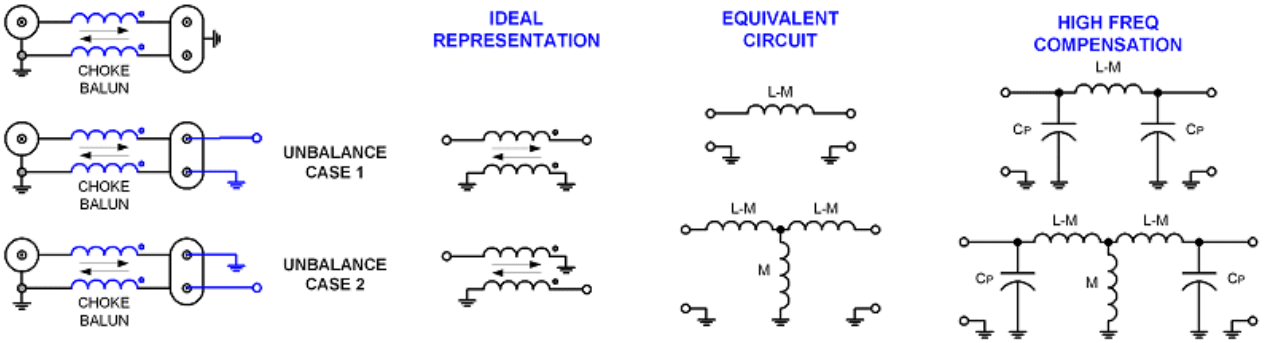

Fig.9 High frequency compensation

and both ports have low frequency/DC shorts. Series capacitors can be used to form a high pass filter response. With this high pass compensation the low frequency limit of the balun can be extended.

High frequency compensation is shown in Fig.9. In some cases the odd mode characteristic impedance can be lowered slightly to extend the bandwidth of the choke balun. As before, the two extreme external unbalance cases are considered. For high frequency performance, case one sets the limit. The series inductor can be compensated with shunt capacitors in a lowpass *pi* or an allpass lattice network.

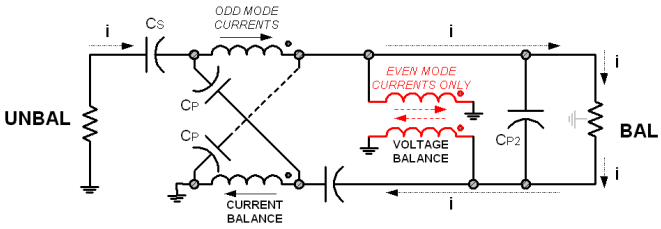

Fig.10 Compensated 1:1 balun circuit

Fig.10 shows a fully compensated choke balun cascaded with a voltage inverter to form a complete 1:1 balun. In 2007 we used a configuration like this to achieve under 0.5dB of loss over the 800 MHz to 2 GHz range. A 3D view of a laminate media realization of this balun is shown in Fig.11. Broadside coupled lines are used (layers 1 and 2) to form the elements. This provided the basis for the output match in a power amplifier that spans the 1.3 octave range with good linearity and PAE.

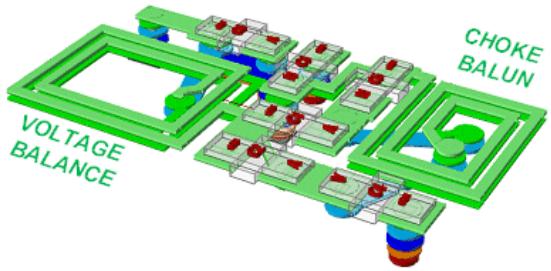

Fig.11 Laminate 3D view of compensated balun

The balance performance of the balun is excellent. One indicator of this is a pair of back-to-back measurements, from single-ended to balanced and back to single-ended. The two cases differ in the sense of the balance interconnect at the cascade interface is reversed for one case. If some imbalance

is present, then one case will be favored. Both were observed to be virtually identical.

VI. Balanced Impedance Transformation

Next we consider the topic of impedance transformation between balanced loads. Balanced to balanced (balbal) transformers are necessary within a pushpull amplifier as part of the interstage network. As before, transmission line type structures will be presented. Later, it will be seen that balanced transformers paired with choke baluns can be used to form very good impedance transforming baluns.

The most commonly used balanced transformer is the Guanella (named after its originator). It provides a 4:1 impedance transformation from a pair of transmission line unit elements. This structure is shown in Fig.12. Common to all transmission line transformer structures, energy is transferred by both

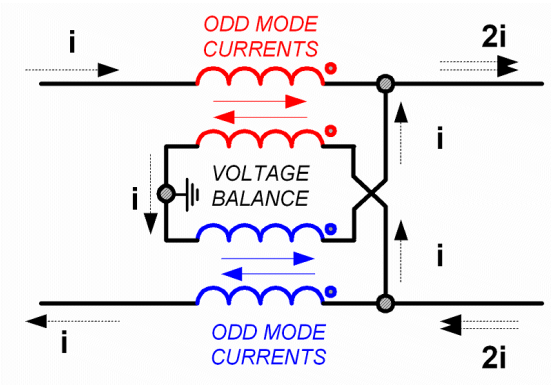

Fig.12 Guanella 4:1 balanced transformer

a conducted path and through flux coupled unit elements. Once again, as with the Ruthroff single-ended analysis, a current is assumed. In this case it is a differential mode current, I, applied to the port on the left. The coupled line unit elements require equal and opposite directed currents as illustrated in Fig.12. The right hand port clearly has a differential mode current of 2i. Conservation of energy leads to the conclusion that this structure provides a 4:1 impedance transformation.

The common mode behavior of the Guanella can be seen in Fig.13. In phase, common mode, currents are assumed/applied to the port on the left. Coupled line unit elements route these currents to the center ground node. If this node is not grounded, it provides a common mode port.

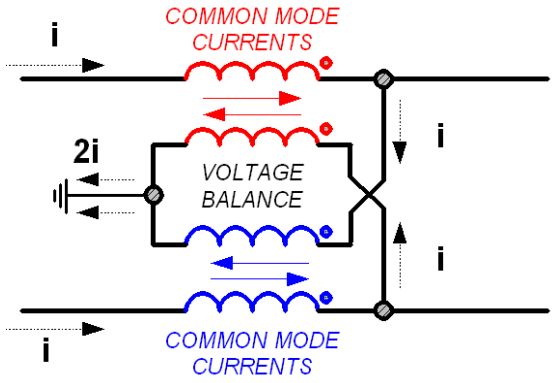

Fig.13 Guanella common mode current flow

In fact, this structure is a 4-port hybrid similar to a wave-guide “magic-T”. To see this, we associate the two left side terminals as the two side ports, the center tap as the common mode port, and the right hand port is the differential port.

If the Guanella schematic is re-drawn, it’s relationship to a balanced auto-transformer can be seen. Consider the two cases shown in Fig.14. Topologically, the Guanella is the same as a conventional auto-transformer. The primary

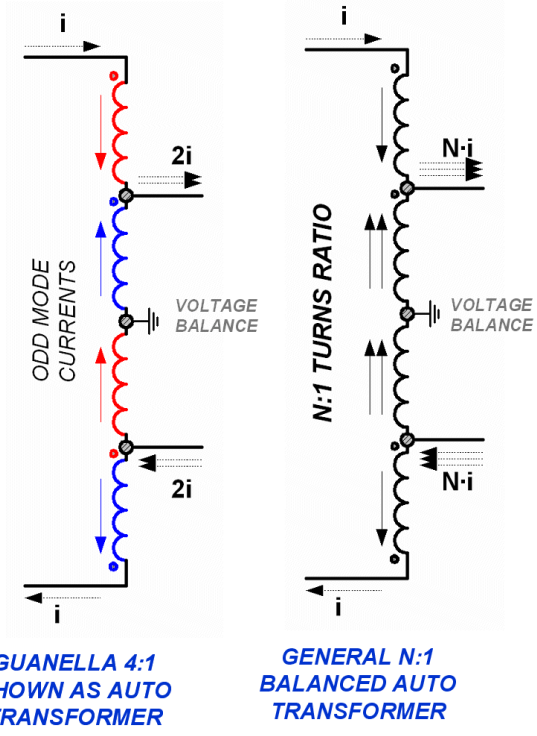

Fig.14 Guanella relationship to autotransformer

difference is in the magnetic coupling. The color coding from Fig.13 is carried over into Fig.14. Note that each outer inductive leg is coupled to an inner segment on the other side. The general auto-transformer is does not have this segmented coupling. The available impedance ratio is another difference. The Guanella is a 4:1 balanced transformer, while the auto-transformer can be set to any ratio. The turns ratio is set the fraction of the total inductance associated with low impedance taps. The impedance ratio is the square of the turns ratio. Both the auto-transformer and the related special case, the Guanella, offer better bandwidth and loss performance that strictly flux coupled transformers. The tapped inductor is more tightly coupled than separate windings, and the conducted path currents are reasons for this.

Like the voltage inverter in the 1:1 balun, the auto-transformer and Guanella provide a voltage balance when the center tap is RF grounded. This leads one to an impedance transforming balun by replacing the voltage inverter, in Fig.10, with an auto-transformer or a 4:1 Guanella. This can be seen with compensation in Fig.15. Of course, the Guanella could be replaced

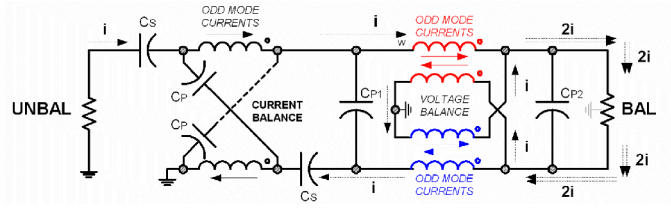

Fig.15 Compensated 4:1 balun circuit

with a different ratio auto-transformer. Non-ideal behavior of the transformer, such as leakage inductance, can be compensated by adding shunt capacitors at both high and low impedance sides. These are labeled Cp1 and Cp2 in Fig.15.

Guanella transformers can be realized in laminate media by forming coupled line unit elements with broadside coupled traces on layers 1 and 2. This can be seen in Fig.16. If the low impedance taps are separated, a modified Guanella structure results. This is also illustrated in Fig.16.

The addition of a compensated choke balun, as indicated in Fig.15, leads to practical power amplifier output matching networks. We have significantly reduced the size of the laminate footprint by stacking the balanced transformer with the choke balun. This can be seen in Fig.17, where the coupled lines for the choke balun are laterally offset in layers1 and 2, followed by a vertical and lateral offset to traces in layers 3 and 4.

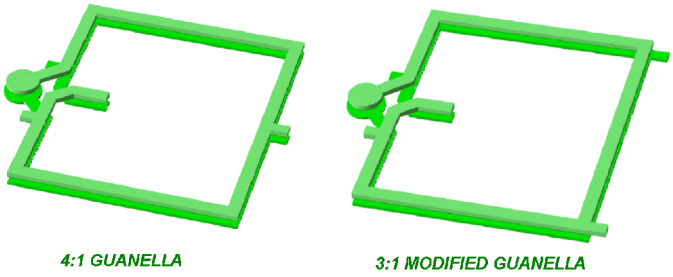

Fig.16 Laminate 3D view of 2-layer balanced (balbal) transformers

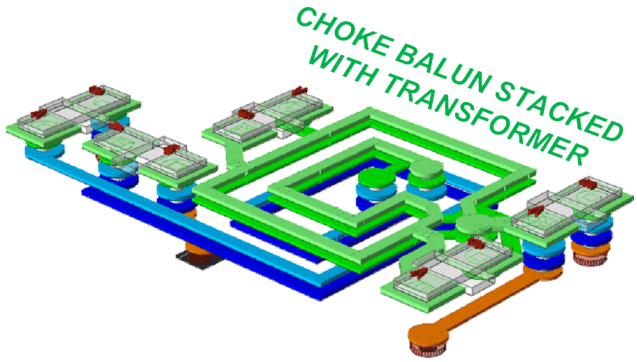

Fig.17 Laminate 3D view of output match (modified Guanella and choke balun)

For yet lower impedance levels a 9:1 auto-transformer can be used with a choke balun. An example of a 9:1 balanced transformer, realized in the top 3 layers of metal of SEMCO's 6 layer process is show in Fig.18.

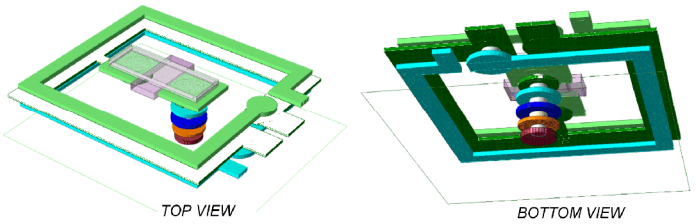

Fig.18 Laminate 3D view of 9:1 auto-transformer

When the 9:1 balanced transformer from Fig.18 is cascaded with a compensated choke balun, the output network shown in Fig.19 is obtained. The choke balun is realized in a broadside coupled pair of lines in layers 1 and 2.

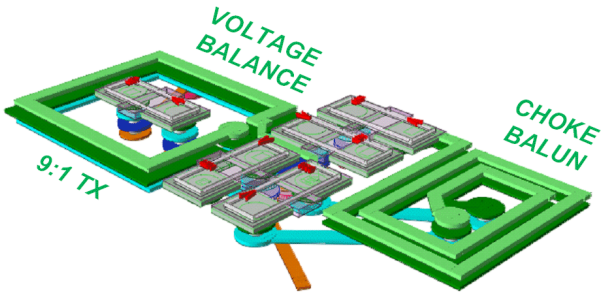

Fig.19 Laminate 3D view of 9:1 output match (auto-transformer and choke balun)

VII. Laminate Development Techniques

A brief discussion of laminate media development techniques for pushpull output matching networks is next presented. Figs. 11, 17, and 19 all illustrate output matching structures with various transformation ratios. One common attribute is coupled line unit elements are all realized in the upper layers of the metal/dielectric stack. The reason for this is coupling coefficient. The transmission line mode between the conductors is used for propagating desired signals. The characteristic impedance in this mode is primarily dependent on line width and vertical spacing. The parasitic transmission line mode between either conductor and the backside ground is responsible for limitations in coupling coefficient. Since we don't have symmetric coupled lines, a discussion in terms of even and odd mode characteristic impedances isn't precisely correct [5]. The correct mode impedances are called π and c. *The important point is that the ratio Zoe/Zoo, or for asymmetric cases Zoc/Zoπ must be large for good coupling.* In a vertical stack of metal and dielectric layers, the distance to the backside ground must be large compared to the separation between the conductors.

In order to accurately represent the circuit behavior of the laminate structure, electromagnetic simulation is necessary. Multiport S-parameter files are loaded into a circuit simulator for analysis of amplifiers. Surface mount component interfaces are best represented by horizontal differential ports. As structures become compacted, unintended coupling to adjacent lines becomes significant. One must consider alternate cases and run comparison simulations. This can be tedious; but, it is necessary for compact structures with high performance. An example of such a structure can be seen in Fig.17.

VIII. Integrated Baluns and Balbals

In the previous section low loss baluns realized in laminate were presented. Because losses in the output network of a power amplifier are so significant in setting (or limiting) it's overall performance level, the output baluns were realized off chip. Lower cost is also a factor in this choice. The input balun and the interstage transformer are not severely constrained to the same extent by loss. Both of these functions have been successfully integrated into the power amplifier chip.

The input balun is similar in form to an impedance transforming balun that was developed on laminate media. It consists of a choke balun cascaded with a Guanella balanced transformer. The Guanella in the input balun is oriented to provide a transformation to higher impedance for driving the bases of the first stage HBT cells. Fig.20 shows this both in schematic form and in layout. The coupled lines in each of the unit elements are realized as broadside coupled (overlay) traces in metals 1 and 2.

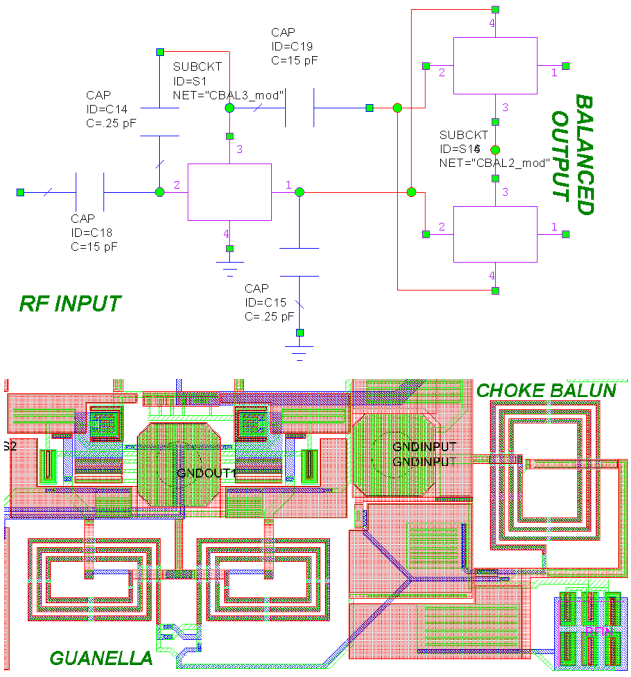

Fig.20 Integrated input balun (choke balun and Guanella)

A Guanella is also used in the cellular band interstage match between the final amplifier and the driver stage collectors. In the PCS interstage, a pair of cascaded Guanella transformers is used to

provide a 16:1 transformation. As with the input balun, the interstage elements are integrated as broadside coupled lines in metal layers 1 and 2. The cellular band interstage transformer can be seen in Fig.21.

IX. PUSHPULL POWER AMPLIFIERS

Each of the critical baluns and transformer elements necessary to configure a pushpull power amplifier has been discussed. Several power amplifiers, configured from these elements, will next be presented. Depending on desired bandwidth, the output choke balun compensation may be simplified. For example, exclusive cellular band operation permits elimination of the high frequency compensation capacitors, while the 1.3 octave amplifier requires all four capacitors in the choke balun compensation.

Fig.22 presents a schematic of a cellular band pushpull power amplifier. This is a version-01 circuit that is useful to communicate the primary circuit features. Some later enhancements such as specific common mode terminations for receive band noise and 2nd harmonic will be discussed separately, later

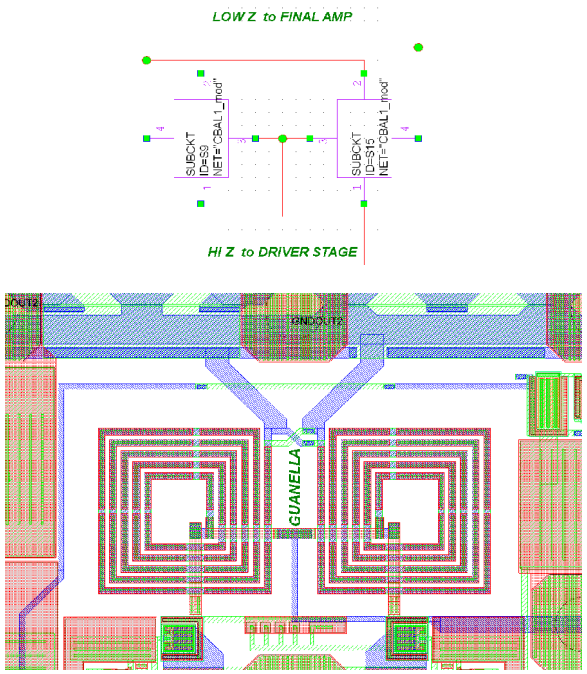

Fig.21 Integrated interstage 4:1 transformer

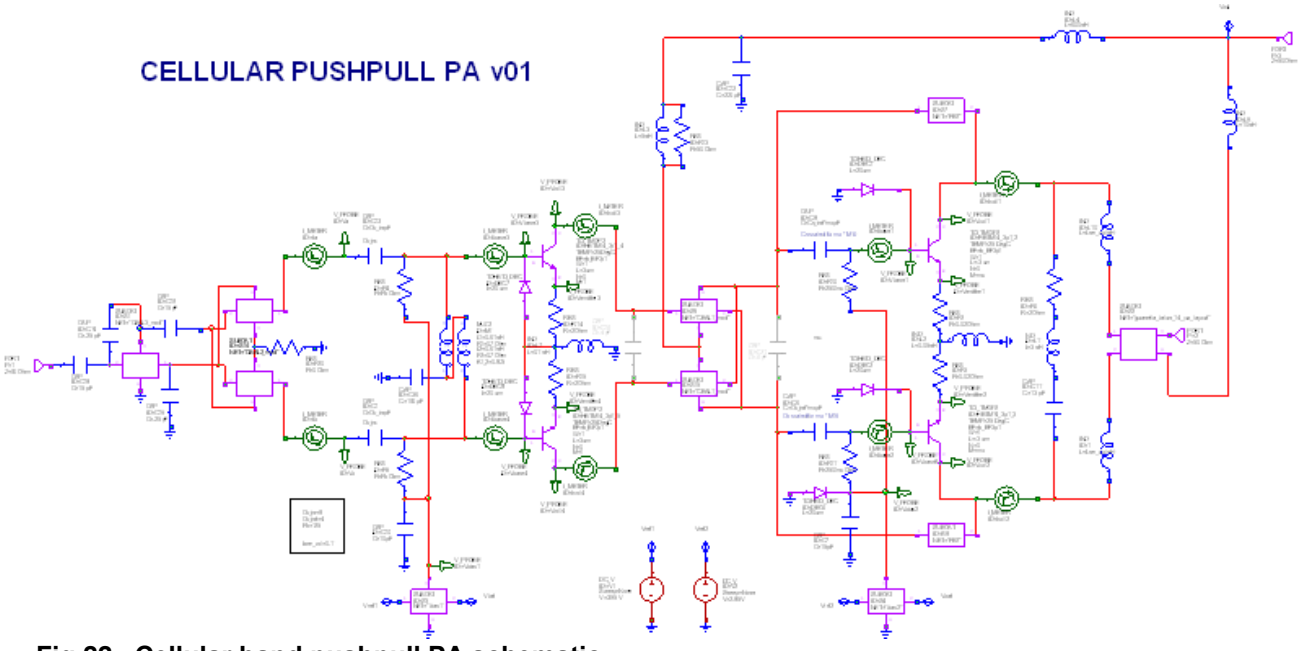

Fig.22 Cellular band pushpull PA schematic

in this paper. The input balun, interstage transformer, and output balun (4-port S-parameter block) can clearly be seen in relation to the driver and final amp transistors.

The driver stage consists of a pair of 335 um^2 mesh (fishbone base) devices. A 1Ω emitter resistor at each device provides signal degeneration in addition to some of the overall ballasting. The remainder of the stage's thermal stability is provided by the base resistors in the bias circuit path. These must not be set to a value less than 65 Ω for thermal stability reasons. By tailoring the size of this series resistance to balance linearity performance between modes, one can achieve an optimum trade-off point between EDGE and UMTS.

The distortion mechanism dominant in UMTS ACLR is different than EDGE 400 KHz ACPR. Higher order IMD terms are more significant in the EDGE case. This leads to a desire for the bias circuit to not be a voltage source. UMTS, on the other hand, performance favors a lower impedance bias interface. The optimum interface to each of the two cells is somewhere between 95 Ω and 150 Ω, depending on mode performance preferences. We reported this bias source impedance relationship to higher order vs. lower order distortion products in our earlier "Plain Jane" development with NCDMA, where we saw a trade-off in ACPR vs. AltCPR dependent on the base ballast resistor value in stage one.

Bias circuits are conventional closed loop circuits that are very similar to those found in the "Plain Jane" amplifiers. One of the clear advantages offered by pushpull operation is the natural isolation between drive RF and bias circuits. Bias is fed in a symmetric common mode path. Differential mode signals are "balanced out". This advantage is significant, especially for linear operation.

The series RLC trap between the output stage collector connections is tuned to the 3rd harmonic. This provides some benefit to linear mode performance. It is possible because the 3rd harmonic is in the differential mode.

The final amplifier has feedback blocks connected between collector and interstage, on each side. These blocks are tuned to have minimal effect in the desired operating band; but, to substantially reduce gain out of band. The circuit for these 2-port blocks can be seen in Fig.23. The parallel LC resonates in the operating band. At resonance, the high impedance minimizes the feedback effect. At frequencies out of band the feedback is RC and much more aggressive. This is especially important

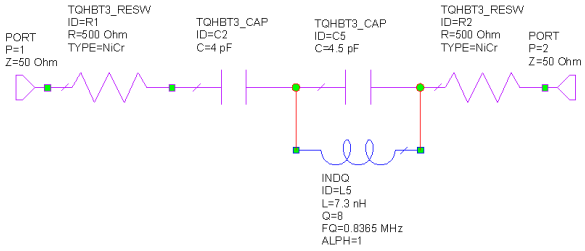

Fig.23 Feedback in cellular output stage

at lower frequencies where device gain is greater and stability is more of a concern. Rather than lumping the series resistance on one end of the network, it is split into two resistors, one at each end. The transfer characteristic is the same in both cases; however, the terminal reflection behavior will be different. Consider a case where the feedback connection from the collector is routed through the series DC blocking capacitor followed by the parallel resonator and then the series resistor before connecting to the base capacitor. The interconnect inductance, capacitor footprint C and the resonator footprint C all cause a shunt capacitive susceptance perturbing the collector tuning. This could easily be an unbalancing effect due to layout routing and placement constraints. It is much safer to isolate the connection at both ends of the feedback block from possible unbalance and detuning with a large series resistor. For this reason, the feedback resistor is split into segments at each end of the network.

A series RLC can be seen between the differential output nodes of the PA IC. This provides a means of terminating the 3rd harmonic that also resides in the differential mode. This technique allows linearity and PAE to be improved in our cellular PAs. The 3rd harmonic termination is relatively insensitive with the worst case performance occurring when it views an open circuit.

The 2nd harmonic termination must be a short circuit or minimally inductive. As long as the output matching network meets this requirement, the space between the differential output pads (or posts) can be used for a 3rd harmonic trap. If the 2nd harmonic provided by the output match is not sufficiently close to a short, then a common mode short must occupy that space on the die. A more detailed discussion of Fourier boundary conditions for optimum pushpull performance will follow subsequently in this paper.

The schematic in Fig.22 does not show an important aspect of the final stage array of cells and their interface manifolds. Consider the photo shown in Fig.24. The output array consists of 24 cells. They are grouped in pairs where adjacent pairs are driven out of phase. In a manner similar to the "Plain Jane", the base feed manifold is comprised of low characteristic impedance transmission lines formed from metal-dielectric sandwiches (metal-2 / BCB / Metal-1). These structures provide low inductance

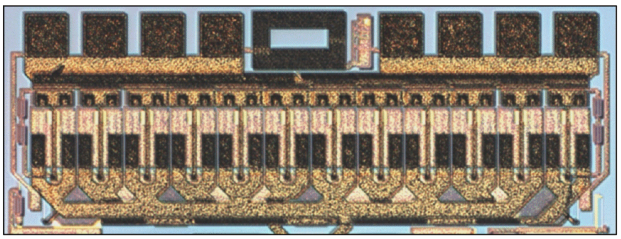

Fig.24 Differential output array

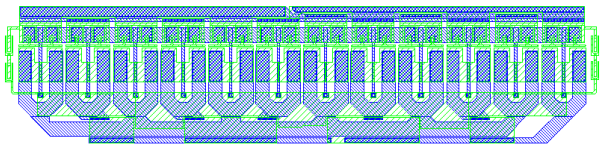

Fig.25 Interleaved input manifold

distribution networks for distributing base drive currents. By interleaving the feed connections between alternate pairs of cells, odd mode emitter currents flow laterally between adjacent pairs of emitter nodes. This short distance represents approximately 28 pH (at each interface). The overall odd mode emitter inductance is on the order of 1 pH ! This provides a significant gain advantage over conventional single-ended arrays. In the common mode an effort to provide a uniform emitter return across the array, since stable behavior in that mode is also necessary. Fig.25 provides a clear view into the interleaved base feed.

In Fig.22, the first stage transistor bases are connected to a voltage inverter (recall Fig.6). This element is intended to have little effect to the desired pushpull operation. It presents a high odd mode impedance to the circuit. In contrast, common mode voltages are short circuited to the center tap. For linear mode receive-band noise performance, the first stage plays a strong role. It is quite important to provide a low impedance path for low frequency noise currents from the input stage transistor bases to ground. This prevents efficient up conversion of noise from baseband to receive band (conversion offset from transmit frequency).

X. Optimum Fourier Boundary Conditions

A detailed analysis of output stage I/O tuning trade-offs was performed in both PCS and cellular bands. The results are plotted in Fig.26. Both cases were run for Vcc=2.5V. Three performance modes were tracked throughout the many cases considered: UMTS, EDGE, and saturated (for GSM). Fundamental and 3rd harmonic tuning was performed in the odd mode and 2nd harmonic terminations were in the even mode. All other cases (odd order in even mode and even order in odd mode) were terminated in an open circuit. Fourier terminating impedances representing Fundamental, 2nd, and 3rd harmonics are labeled 1,2, and 3, respectively.

Fundamental frequency output tuning was no surprise. For higher voltage operation, the real loading level increases approximately with the square of the supply voltage scaling. Similarly, the shorted 2nd harmonic load condition was expected for good linear mode performance. The output 3rd harmonic tuning was optimum near a short with some inductive reactance. Sensitivity to 3rd harmonic tuning is mild, as long as the open circuit condition is avoided.

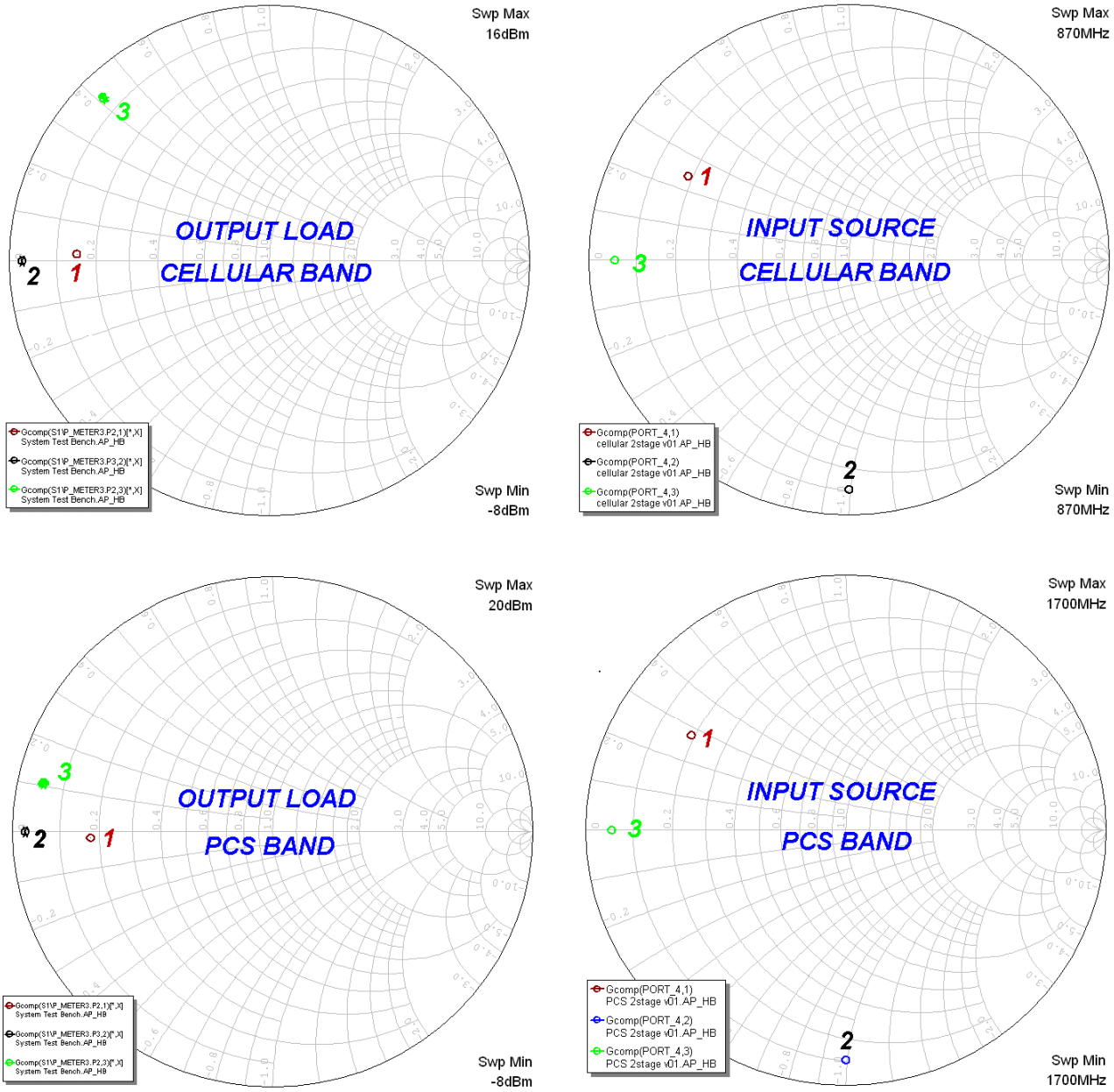

Fig.26 Optimum Fourier boundary conditions

Apparently this leads to too much 3rd harmonic voltage peaking. The 2nd harmonic load tuning is much more sensitive than that of the 3rd . Fundamental frequency input tuning can be thought of as providing two functions. The source's inductive susceptance cancels the capacitive behavior of the device. The real part provides a basis for broadband power transfer. The real part tuning offers an important trade-off. This is between gain and linearity. The lower the real part of the source, the greater the gain until conjugate match is achieved. Generally, increases in the real part of the source lead to greater linearity at the expense of gain. This is not surprising when one considers the linearising effect of a series resistor with a PN junction. In this way, the input current loop is influenced to a lesser extent by the nonlinear behavior of the emitter-base junction. The 2nd and 3rd harmonic tuning targets for both bands are similar: a short for 3rd harmonic and capacitive for 2nd harmonic. Sensitivity to input harmonic termination is moderate. It is important to avoid a short circuit 2nd harmonic source or an open circuit 3rd harmonic source termination.

XI. Laminate Impedance Matching Performance

Now that fundamental and harmonic load targets have been established, performance of several matching networks can be assessed. High Vcc matching networks, intended for use with a buck-boost DC-DC converter, will be considered in both cellular and in PCS bands. As before terminating impedances representing Fundamental, 2nd, and 3rd harmonics are labeled 1,2, and 3, respectively.

Fig.27 shows the match and loss performance from the initial (ver.0101) cellular and PCS laminates.

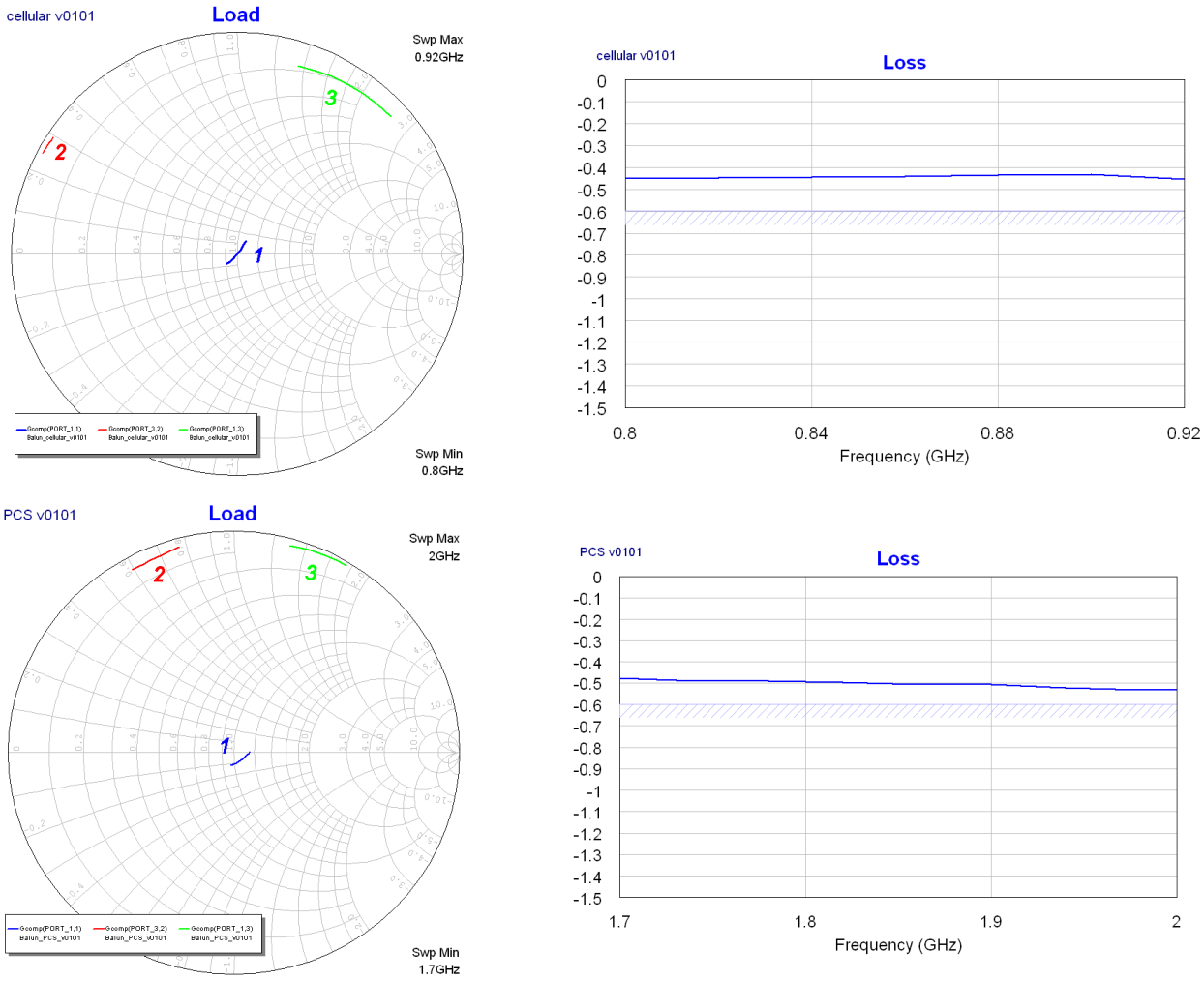

Fig.27 Cellular and PCS laminate match (v0101)

While the load across each band is well controlled and losses are relatively low, the 2nd harmonic is not shorted. In the cellular case the 2nd harmonic termination has a small enough inductive reactance to be usable, as is. The PCS 2nd harmonic termination has twice the reactance as the cellular case. This is too large. The 3rd harmonic terminations in both bands are inductive and similar. The range of 3rd harmonic terminations to be avoided are near an open, especially capacitive values near open circuit. This 3rd harmonic behavior could be improved but it is usable, as is.

The cellular PA chip (Fig.22) that was discussed previously, uses a 3rd harmonic trap to move the termination at or near (inductive) a short. This LC network can be seen in Fig.24, between the differential output pads. Recall, the 3rd harmonic is in the differential (or odd) mode. This series LC trap also provides additional attenuation to 3rd harmonic output levels. The result of this can be seen by comparing Fig.28 to the cellular load case in Fig.27. Rather than setting the 3rd harmonic termination to a short, it has been set slightly inductive to match the optimum target shown in Fig.26.

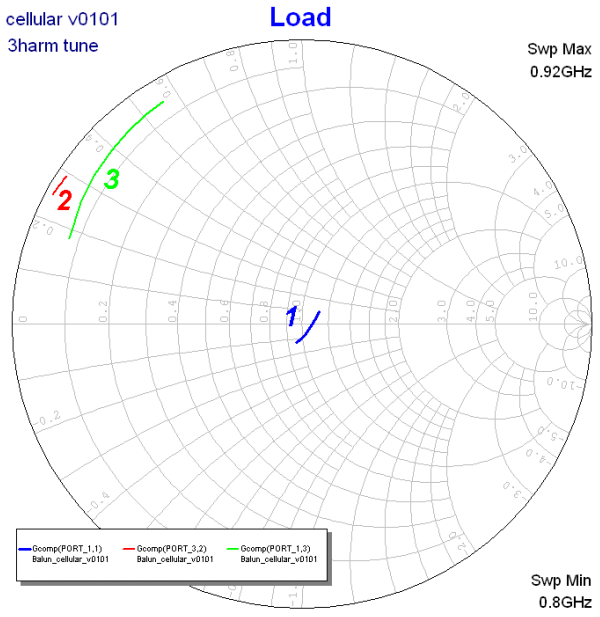

Fig.28 Cellular match with 3rd harmonic tuning

The PCS laminate match shown in Fig.27 requires some improvement in the 2nd harmonic termination. Since the 2nd harmonic resides in the common mode, a voltage inverter (see Fig.6) can be used. This can be conveniently placed between the differential output pads as an alternative to the 3rd harmonic trap that was used in the cellular band PA. The result of

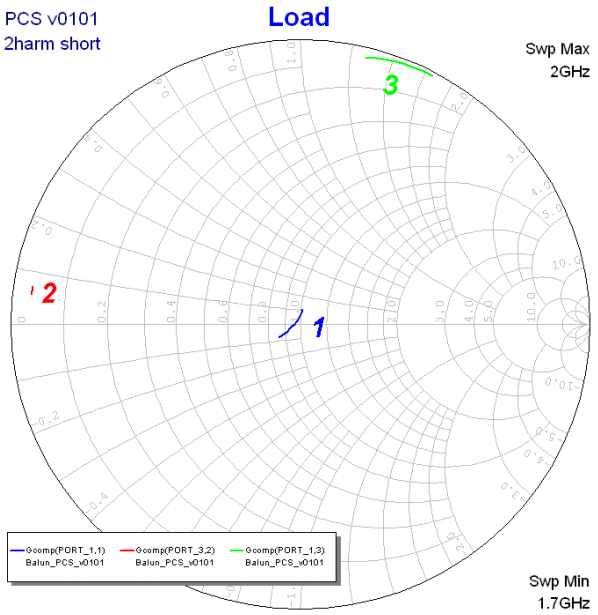

Fig.29 PCS match with common mode short

this can be seen by comparing Fig.29 to the PCS load case in Fig.27.

Whether to correct the 2nd harmonic with a common mode short or to tune the 3rd harmonic, as in the cellular case, depends on the relative harmonic tuning error in the original laminate match. In the cellular case, the 2nd harmonic termination is close enough to a short for usable performance. We are currently investigating the use of a common mode

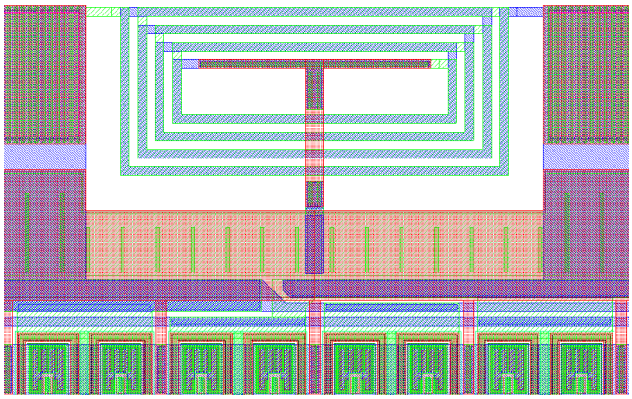

Fig.30 PCS PA integrated 2nd harmonic short

short in the cellular case. In the PCS laminate, there is no question that the 2nd harmonic tuning error is a much greater issue than that of the 3rd harmonic. Fig.30 shows a voltage inverter used to provide a common mode short in a PCS PA. The center tap node is returned to a large bypass capacitor that is distributed along the output cell array.

XII. Laminate Layouts for Pushpull PAs

The cellular and PCS multimode PA module laminate layouts (high Vcc cases) are shown in Figs.31 and 32. Each design is for full bandwidth operation: 824 MHz to 915 MHz cellular and 1.71 GHz to 1.98 GHz PCS. The laminates for both bands are very similar.

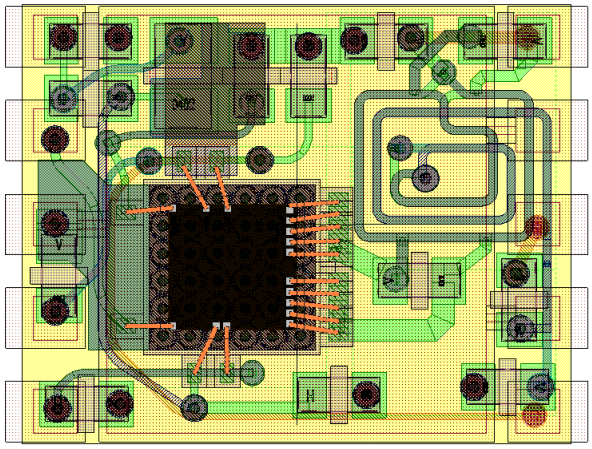

Fig.31 Cellular multimode pushpull PA layout

The primary difference is in the size of the output balun structure. These layouts embody the cases that were discussed in the previous performance section. Both output structures are modified Guanella transformers stacked with choke baluns, as illustrated previously in Fig.17. Layouts were done in the AWR environment using MAT051 PDK modified for SEMCO's 50um/50um (line width/gap) six layer rules. Both are DRC compliant. Prototype development work has been with wire bond chips that use substrate vias. Ultimately, production chips will likely be done with a flip-chip interface.

In addition to high Vcc operation (for buck-boost DC-DC), low Vcc operation has been explored in the cellular band. A reduced load impedance is necessary to support the same power levels as the

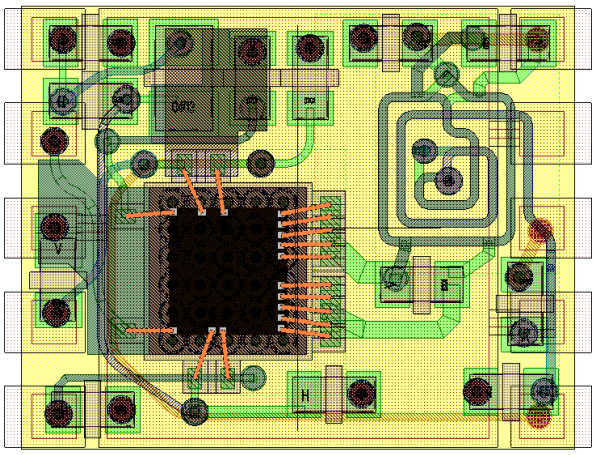

Fig.32 PCS multimode pushpull PA layout

DC supply is lowered. The 9:1 auto-transformer structure that was shown in Fig.18 was used in the low Vcc design. Fig.33 shows a cellular layout of this type. The cascaded choke balun can be seen in the lower left corner of the layout.

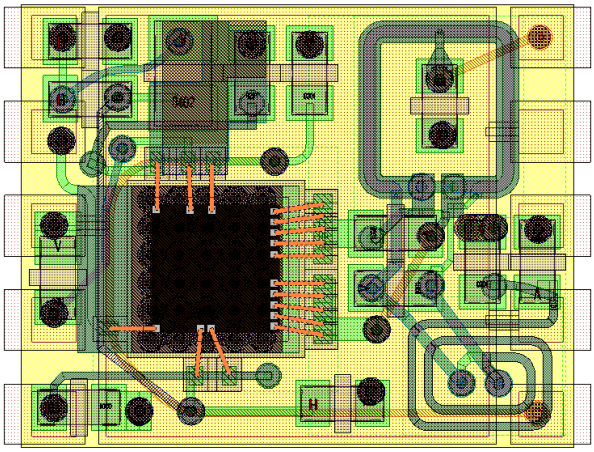

Fig.33 Cellular multimode low Vcc PA layout

It is possible to realize good performance over a very wide bandwidths with pushpull configured PAs that operate at high supply voltage. Our first exploratory investigation of pushpull operation was a PA that spanned 1.3 octaves from 800 MHz to 2.0 GHz. This operated at a supply rail of 5.5 V. Good WCDMA performance was seen in the two cellular and in the three PCS bands contained in that range. In general, as the transformation ratio is increased, the bandwidth performance is traded off. This is due to the practical limitation in coupling coefficient in the

transmission line unit elements. For this reason, the 1.3 octave PA was configured with a 1:1 balun. In order to provide full WCDMA power, 5.5 V is needed. The 1:1 balun consists of a voltage inverter cascaded with a choke balun similar to the circuit shown in Fig.10. This PA can be seen in Fig.34, as a flip chip layout. The voltage inverter occupies the upper right corner while the choke balun can be seen in the lower right corner of the layout.

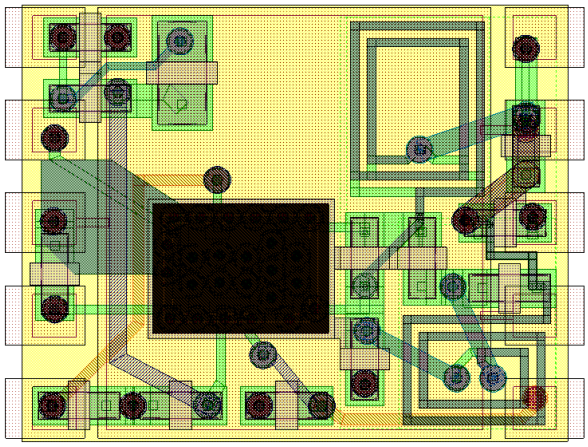

Fig.34 Wideband (1.3 octave) pushpull PA layout

XIII. Measured Performance

Currently, the PCS amplifier shown in Fig.32 is under development and performance data is not yet available. The cellular amplifiers shown in Figs. 31 and 33 are more mature. For example, the high Vcc PA (Fig. 31) operates in GSM, EDGE, and WCDMA at supply voltages of 4.6, 3.9 and 3.5, respectively. Outstanding performance is obtained across several cellular bands spanning the frequency range from 824 MHz to 915 MHz. This multiple mode and multiple band amplifier capability is sometimes called a "*CONVERGED PA*".

Typical power performance in GSM is better than +34.5 dBm with 63% power added efficiency (PAE). WCDMA PAE performance is typically 40% at output levels of +28 dBm (or greater) and -40dBc ACPR. EDGE PAE is similar to that of WCDMA at power levels of +28.5 dBm. The power efficiency performance of this amplifier in each of the modes is better than most single mode amplifiers. This approach provides enough margin in PAE to enable use of a Buck-Boost DC-DC converter with a competitive overall efficiency. As was stated in the introduction, superior PAE is a result of both the increased load impedance from pushpull operation and of the elevated supply voltage. Both these factors also aid in achieving true multimode operation from a single PA. The simplicity of mode changes by changing only the supply voltage is very attractive. This approach also allows a means of providing high PAE at power back-off by simply reducing the supply voltage. Fig.39 shows the overall PAE measured with a prototype NSC "Talon" Buck-Boost converter and our converged PA as a function of battery voltage. It is important to note the relatively flat insensitivity in PAE. In contrast, a PA designed optimally to operate at 2.5V would be significantly challenged to do better than this. Another advantage available to a PA with a Buck-Boost converter is a straight forward path to load insensitivity; but, that's a topic for another paper.

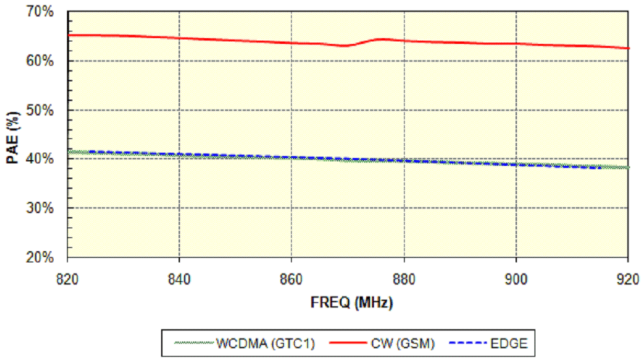

Fig.35 PAE performance in all modes

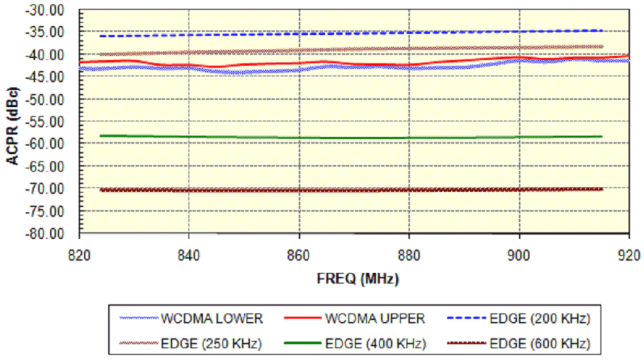

Fig.36 ACPR performance in WCDMA and EDGE

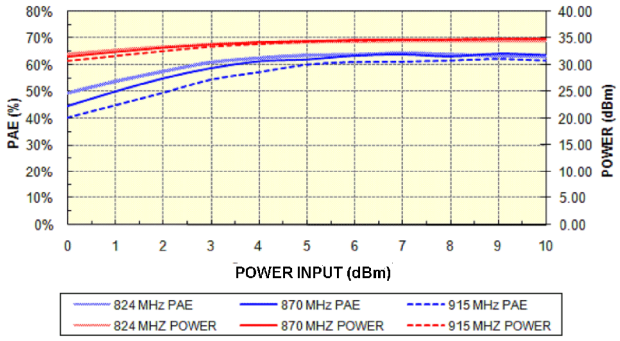

Fig.37 GSM PAE and power output vs input

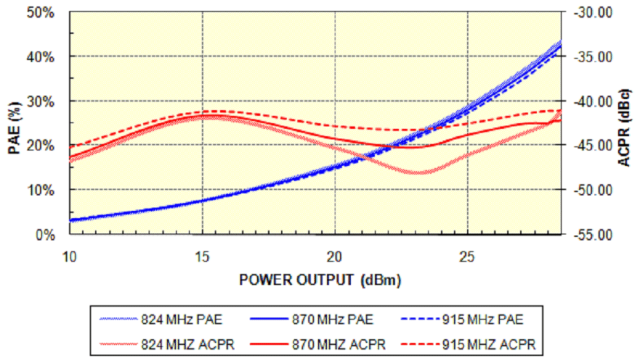

Fig.38 WCDMA PAE and ACPR vs power output

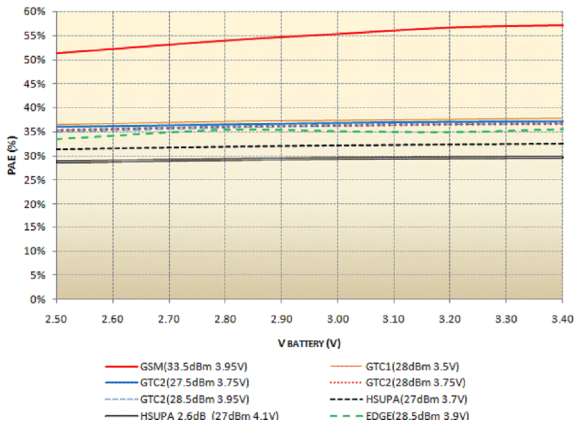

Fig.39 PAE with DC-DC converter vs Vbattery

It is useful to put the performance of this PA in perspective by comparing it with our best single-ended WCDMA PA, the "plain-Jane" (Dec.2007). Fig.40 displays ACPR of both PAs vs power output at three different DC supply voltages. The modulation in all cases is HSUPA-2.6 dB backoff. This was selected to aggressively challenge the linearity performance. From the -40 dBc ACPR limit, it can be seen that both amplifiers are loaded for similar power vs Vcc. At supply voltages of +3.5, +4.0, and +4.5 V, output levels of +26.5, +27.5, and +28.5 dBm are associated with -40 dBc ACPR. From Fig.41 the improvement in PAE in the pushpull amplifier is observed to be approximately 5%. An increase in gain of 2.5 dB is also typical.

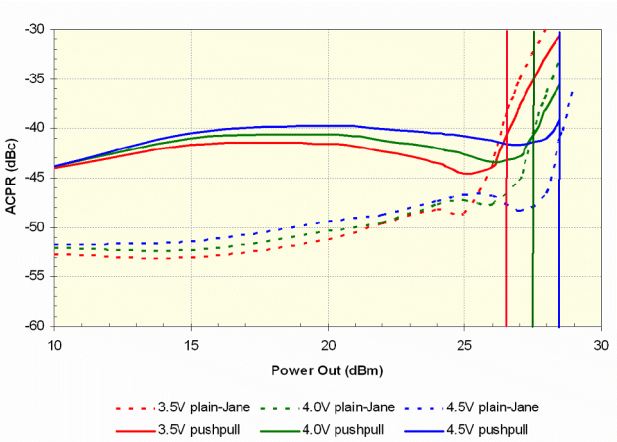

Fig.40 Pushpull to "plain-Jane" comparison shows similar loading for power vs ACPR

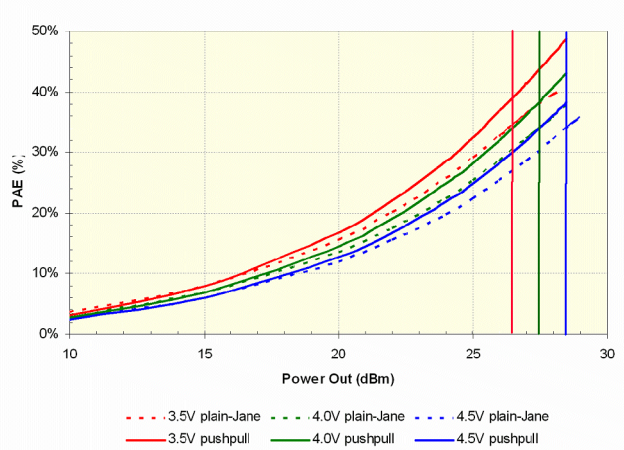

Fig.41 Pushpull to "plain-Jane" PAE comparison

XIV. Other Considerations

Stability in general and into mismatch are important aspects of PA design. A small signal Rollett or Linvill check is not sufficient to insure a stable power amplifier. For example, if the final stage array of cells is electrically distributed over more than a half wavelength at frequencies where substantial gain is present, an odd mode (transverse direction) oscillation may be possible. This is seen occasionally in Ku band single-ended PAs and can arise without large signal operation. So an undesired odd mode oscillation can be present in an amplifier that is intended for even mode operation. Similarly, a pushpull PA may be susceptible to even mode instability. The additional degree of freedom offered by mode separation in a pushpull PA requires careful attention to both modes. A linear analysis in the differential mode will probably not show instability tendencies in the common mode. A quick (but not conclusive) check of the common mode can be performed by using voltage inverters to couple into that mode and performing a linear stability analysis. If this indicates problems, they are real. If none are apparent, some may still be hidden. The only way to insure stability is to perform a rigorous analysis that considers conditions at each active device, such as the NDF technique of Platzker [7].

Power amplifiers are by nature nonlinear. The behaviors of (RF amplifier) constituent transistors depend on operating signal levels. Consequently, stability can be present at small signal and vanish at large signal. Large signal conditions change with changes in load. Clearly, a comprehensive stability analysis must consider conditions at each device (as in NDF) over a wide range of operating conditions such as power level and load. The best way to address this complicated problem is with an auxiliary generator technique [8].

VII. Conclusion

The development of pushpull power amplifiers for handset applications has been presented. This approach offers superior performance when compared with conventional single-ended PAs.

The key element enabling these amplifiers is a low loss, compact and inexpensive balun output circuit. General transmission line transformer and balun development was discussed. Realization in multilayer laminate media, for output matching was detailed. Integration on chip, for input and interstage matching, was also presented.

Optimum load and source impedances for converged PA operation were presented at fundamental, 2nd and 3rd harmonic frequencies. This was provided in both PCS and in cellular bands.

Performance of laminate media output baluns was compared to the optimum load targets. Harmonic compensation techniques were also given.

A cellular two-stage amplifier circuit was discussed in detail with measured results.

Acknowledgement

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