8 GaAs FET Amplifier and MMIC Design Techniques

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8.1 INTRODUCTION

The objective of this chapter is to present a systematized approach to GaAs FET amplifier design. The broadband design techniques discussed here are also applicable to narrowband amplifier design as an inclusive subset. A two-stage power amplifier design is included as an example. Finally, MMIC (monolithic microwave integrated circuit) realization of lumped element designs is discussed.

With the exception of distributed amplifiers, microwave amplifiers are usually comprised of several GaAs FET devices interconnected with input, interstage, and output impedance matching networks. This is shown conceptually in Fig. 8.1. The specific amplifier application will usually determine the necessary impedance behavior which must be provided by each network. The important point here is that the methodology by which the networks are obtained remains the *same*, *regardless of application*. For example, the techniques that we are about to consider are applicable to both low-noise amplifiers and power amplifiers. They are equally applicable to single- or multistage amplifier design requirements. In fact, they also provide an effective means of insuring optimum narrowband design as well.

In order to see that the network problem for all broadband amplifier applications is really the same, several applications will be now considered. Each case will then be reduced to the (same) problem of obtaining an *LC* network with some desired driving-point impedance behavior.

1. *Low-noise amplifier*. From the optimum noise reflection coefficient ρ_{opt}, the desired matching network driving-point impedance Z_S can be determined

$$Z_S = 50 \frac{1 + \rho_{opt}}{1 - \rho_{opt}}$$

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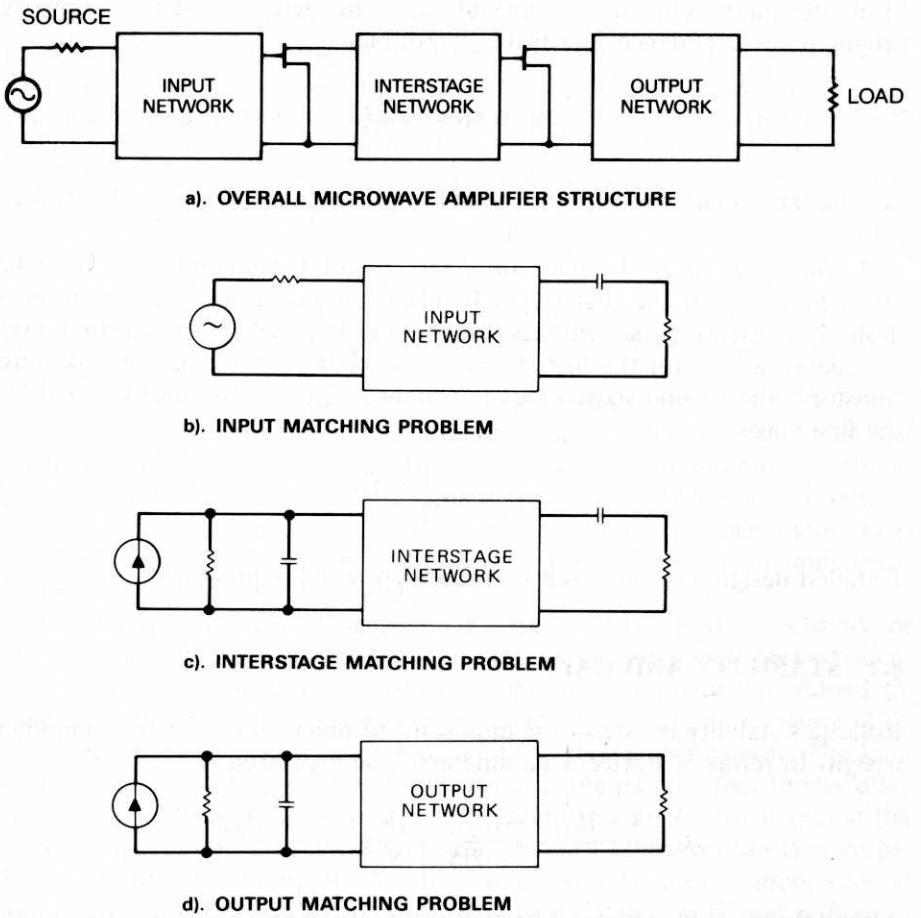

Figure 8.1 Three basic matching problems of a multi stage amplifier.

Hence, the input design requirements are in the desired form. Flat amplifier gain can be achieved by controlled mismatch at the output port of the device. Typically, constant gain circles are plotted for this interface. A desired load impedance Z_L is then determined. Therefore, the output matching network is also specified in the desired form.

2. *Power Amplifier.* Either from load line considerations or load–pull data the optimum load impedance $Z_{L\,opt}$ is determined. The design task is to obtain an output matching network that provides this optimum load impedance behavior. Usually, minimum input port reflection is desired. The device input reflection coefficient S'_{11} is determined:

$$S'_{11} = S_{11} + \frac{S_{12}S_{21}\rho_{L\,opt}}{1 - S_{22}\rho_{L\,opt}}$$

From the input reflection coefficient S'_{11}, the desired matching network driving-point impedance Z_S can be determined:

$$Z_S = 50 \frac{1 + S'^*_{11}}{1 - S'^*_{11}}$$

So, the input matching network design requirements are also in the desired form.

3. *Interstage of High Gain Amplifier.* S'_{11} of the second stage must be matched to S'_{22} of the first stage. If mismatch gain slope compensation is desired, constant gain contours can be used to select the desired load impedance $Z_{L\,opt}$, for the first stage. The interstage matching network must transform the second-stage input impedance Z_{IN} into the desired load for the first stage, $Z_{L\,opt}$:

$$Z_{IN} = 50 \frac{1 + S'_{11}}{1 - S'_{11}}$$

Detailed design examples will be presented in subsequent sections.

8.2 STABILITY AND GAIN

Rollette's stability constant k is important to practical GaAs FET amplifier design. In terms of device S-parameters, it is expressed as

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 - |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{21}|\,|S_{12}|}$$

Although one-port unilateral models (as seen in Fig. 8.27) are frequently used to represent impedance matching requirements, the complete device representation is nonunilateral. Therefore, at frequencies at which useful gain is available, the potential for oscillations must be examined. Even for power amplifier applications, where the device is being operated nonlinearly, small-signal stability should also be considered.

The significance of Rollette's stability constant is that for $k > 1$, the device is unconditionally stable and no combination of load and source impedances can produce oscillations. For this case, simultaneous complex conjugate matching of the FET input and output ports is possible. When this is done, maximum available gain (MAG) results. The expression for MAG is given by

$$\text{MAG} = \frac{|S_{21}|}{|S_{12}|}\,(k - \sqrt{k^2 - 1})$$

If, on the other hand, $k < 1$, some load and source impedances can cause

oscillations. In such cases, the impedance regions to be avoided can be plotted or represented graphically by circular regions on the Smith chart. This method is adequately described in several references [1, 2]; hence, it will not be repeated here. Often, these difficulties are avoided when lossy negative feedback or lossy branch amplitude equalization techniques are employed. The lossy branch technique will be discussed in the two-stage design example of Section 8.4.4.

8.3 *Q*-BANDWIDTH LIMITS ON IMPEDANCE MATCH

Before any attempt to design a broadband matching network, the achievable match performance must first be determined. A common pitfall that the inexperienced circuit designer often encounters is an attempt to obtain matching networks blindly by numerical optimization. If the desired performance level is not achievable, considerable computer and engineering time can be wasted. This section addresses the limits imposed on impedance match performance by load behavior.

The relative reactive to resistive (susceptive to conductive) behavior of the load immittance sets the limits on achievable broadband performance. This behavior is sometimes described in terms of a parameter called load-Q. Bode [3] showed that the integral of return loss is bound by a constant. This constant is dependent on the behavior of the reflection function. The load that was initially considered by Bode was a simple parallel RC. In this case, the match performance limit can be described in terms of load-Q and the complex frequency location of matching network reflection function zeros. Several years later, Fano [4] extended Bode's work to address more general cases. For our purposes here, a detailed look at Bode's work will suffice. In addition to the parallel RC case that Bode considered, we will show that the circuit-dual (series RL case) also yields the same results. So, all single reactance absorption lowpass cases are covered. These results can then be extended to the two-element bandpass cases by the well-known lowpass to bandpass transformation.

The two cases that will now be considered are illustrated in Fig. 8.2. An LC matching network that absorbs to complex valued load behavior and provides an impedance-matched filter response to the R_0 source is desired. Matching networks are filter structures. However, a filter that provides a low reflection match between a resistive source and load is not necessarily a matching network. The additional requirement that is imposed on matching networks is reactance absorption at one or both sides of the structure. Typical filter responses have zero flat-loss (offset) due to reflection zeros on the imaginary axis. Since matching networks have additional constraints placed on them, additional degrees of freedom in the realization are required. General placement of reflection zeros allows this freedom. The

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