POWER MOSFETs versus BIPOLAR TRANSISTORS

Prepared by: Helge O. Granberg
Sr. Staff Engineer

What is better, if anything, with the power FETs if we can get a bipolar transistor with an equal power rating for less than half the price?

Several manufacturers have recently introduced power FETs for RF amplifier applications. Devices with 100 W output capabilities are available for VHF frequencies and smaller units are made for UHF operation. All are enhancement mode devices, which means that the gate must be biased with positive voltage (N channel) in respect to the source to “turn it on.” Early designs were so called V-MOSFETs, where the channel is in a V-groove. The V-groove must be etched with a special process, and the silicon material must have a different crystal orientation from the material normally used for bipolar transistors. The difficulty of the etching process in production has led to the development of other types of channel structures such as HEX and T, which are still vertical channel structures, but V-groove is eliminated, and the gate is on a straight surface. Thus, for an equal gate periphery, more room on the surface is required. Japanese manufacturers seem to favor geometries with horizontal channels. They are similar to small signal MOSFETs with a number of them paralleled on one chip. This technique represents even more wasteful use of the die surface than HEX or TMOS. Typically a power FET requires 50 to 100 percent more die area than a bipolar transistor for equal power output performance. For TMOS the number is about 50 percent. This is mainly due to the higher saturation voltage, but the geometry also gives some 30 percent less gate periphery than available base area in bipolar. Since the price of a solid state device is a function of a die size, we get fewer watts per dollar. This is completely opposite from what the industry has been trying to do in the past years with bipolar transistors. So, one may ask: What is better, if anything, with the power FETs if we can get a bipolar transistor with an equal power rating for less than half the price? This is where we come to the purpose of this article, which is to discuss the characteristics of the FET and bipolar device. Both have the same basic geometry, but with some mask changes, one was processed as a MOSFET and the other as a bipolar.

CIRCUIT CONFIGURATIONS

Since the gate of a MOSFET device is essentially a capacitor, which consists of MOS capacitance distributed between the channel and the surface metallization, the input Q is normally extremely high. For this reason, the gate must be de-Q’ed with a shunt resistance or applying negative feedback or a combination of the two. Unless this is done properly, the affect of feedback capacitance (C_{rss}) will result in conditions, where stable operation is impossible to achieve.

<table>
<thead>
<tr>
<th>TABLE A</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bipolar</strong></td>
</tr>
<tr>
<td>Z_{in} RS/XS (30 MHz):</td>
</tr>
<tr>
<td>Z_{in} RS/XS (150 MHz):</td>
</tr>
<tr>
<td>Z_{OL} (Load Impedance):</td>
</tr>
<tr>
<td>Biasing:</td>
</tr>
<tr>
<td>Ruggedness:</td>
</tr>
<tr>
<td>Linearity:</td>
</tr>
<tr>
<td>Advantages:</td>
</tr>
<tr>
<td>Disadvantages:</td>
</tr>
</tbody>
</table>

© Motorola, Inc. 1993
Figure 1 shows a Smith Chart plot of a 150 W MOSFET and a bipolar device using the same basic geometry for comparison purposes. The gate of the FET has been shunted by a resistance of 20 ohms. Without the shunt resistance the input impedance would be a pure capacitive reactance, if package inductances are disregarded.

The input Q is an inverse function of the broadbandability of a device. With the techniques mentioned above, the Q can be controlled to a large degree, but some power gain will be sacrificed, unless only some type of selective negative feedback is employed for that purpose. Amplifiers in the 100 W power level, covering five octaves can be designed, and the limiting factor only seems to be the proper design of the broadband matching transformers.

Due to the lack of base diode junctions inherent to bipolar devices, where the diode forward conductance depends on the drive level, the MOSFET gate impedance varies only slightly with the input voltage amplitude. The gate MOS capacitance should be more or less independent of voltage, depending on the die processing. This is considered one of the advantages with FETs, especially regarding amplitude modulated applications, where a constant load for the driver stage is important. Negative feedback should be limited, since it tends to deteriorate this characteristic. Another advantage is the AGC capability by varying the gate voltage. In common source configuration, depending on the initial power gain, etc., an AGC range of 20 dB is achievable.

Common gate configuration has some advantages, although it is not useful in applications requiring linearity. The load impedance is reflected back to the gate and in effect is in parallel with the source to ground impedance. The total input impedance is more constant with frequency than in common source mode, but varies greatly with output power level and supply voltage. As in a comparable configuration with bipolar transistors, the overall power gain is low, but the unity gain frequency (\( f_{\alpha} \)) extends higher, which makes the common gate circuit attractive at UHF designs. It also has more tendency for parasitic oscillations, since the input and output are in the same phase. The de-Q’ing of the input can be done in the same manner as in a common source circuit, but negative feedback is not as easy to implement. This circuit also exhibits greater power gain versus bias voltage variation characteristics. In applications, where 40 dB to 50 dB AGC range is required, the common gate configuration should be considered.

A common drain configuration represents the emitter follower in bipolar circuits. In both cases the input impedance is high and the load impedance is effectively in series with the input. The input capacitance, (drain-to-gate, or collector-to-base) is lower than in common source or common gate circuits, and several times lower for the FET than bipolar for equal die size. This is due to lack of the diode junction. A MOSFET source follower cannot be regarded as having current gain as the emitter follower. The amplification rather takes place through impedance transformation. Due to the fair amount of input de-Q’ing required, the available power gain is lower than in common source circuit for example. Having less than unity voltage gain, the circuit exhibits exceptional stability, and negative feedback is not necessary, nor can it be easily implemented. Push pull broadband circuits for a frequency range of 2 to 50 MHz have been designed for 200–300 watt power levels. Their inherent characteristics are good linearity and gain flatness without any leveling networks. High power SSB amplifiers are probably the most suitable application for common drain operation. The AGC range is comparable to that in common source, but higher voltage swing is required. It must be noted that the MOS devices used must have high gate rupture voltage, since during the negative half cycle of the input signal, the gate voltage approaches the level of \( V_{DS} \).
LINEARITY ASPECTS

Some literature claims that MOS power FETs are inherently more linear than the bipolar transistors. This is only true up to the point where envelope distortion, caused by saturation, instabilities or other reasons, is not present. It is also a function of the bias current (I\text{DQ}). The FETs usually require higher idling currents than the bipolars to get full advantage of their linearity. Bipolars are usually biased only to get the base-emitter diode into forward conduction, whereafter increasing the bias helps little. Class A is an exception, but the device must then be operated at 20–25 percent of the rated Class AB level.

Probably the main advantage with the MOS power FETs is their greatly superior high order IM distortion performance. This is mainly due to the fact that ballasting resistors are not required with FETs. In bipolar RF power transistors, nonlinear feedback is distributed to each emitter site through the MOS capacitance from the collector. In devices using diffused silicon resistors, this effect is even worse, and caused by additional nonlinear diode capacitance between the collector and the emitters. The high order IMD (9th and up) is actually in direct relation to the ballasting resistor values, which must be optimized for an even power distribution along the die. Too low values would result in a fragile device, and the opposite would, in addition to the IMD problem, result in high collector-emitter saturation voltage and low power gain.

The feedback capacitance, drain-to-gate or collector-to-base for example, also has a secondary effect in IMD. In both cases it is a function of the die geometry, and is usually lower with devices with higher figure of merit, such as the ones made for UHF and microwave applications. A MOS power FET exhibits some five times lower feedback capacitance than a bipolar transistor with a similar geometry. In a bipolar transistor this capacitance partly consists of the collector-base junction, which is highly nonlinear with voltage. This, together with the varying input impedance, generates internal feedback, which is nonlinear and produce high order IMD to some degree. A more noticeable effect is that the low order IMD goes up with reduced drive levels as shown in Figure 6.

This can be related to different turn on characteristics between the two device types. When a bipolar device is biased to Class AB, the bias does not usually, completely overcome the V\text{BE} knee. Thus, at lower signal levels, the remaining nonlinear portion covers a larger area of the total voltage swing. Increasing the bias from the normally recommended Class AB values will help and full Class A should eliminate the problem completely.

![Figure 3. A Typical Common Gate MOSFET Power Amplifier Circuit](image)

![Figure 4. A Typical Common Drain, Narrow Band MOSFET Power Amplifier Circuit](image)

![Figure 5. Two Tone Spectrographs of 300 W PEP, 50 V Amplifier Outputs](image)
a. using bipolar transistors a. and b. with TMOS power FETs. 500 mA of bias current per device was used in each case. Doubling the bias current has a minimal effect in a. but the 7th order products would be lowered by 10–12 dB in b.
Switching mode RF power amplifiers have only become feasible since the introduction of the power FET. Being a majority carrier device, the FET does not exhibit the storage time phenomena, that limits the switching speed of a bipolar. For a given device, the switching speed is mainly determined by the speed the gate capacitance can be charged and discharged. If the capacitance is in the order of several hundred pF, a smaller FET is required to provide the fast charge-discharge switch. For low power stages, bipolars can be used, since the storage time is mainly an inverse function of the ft and device size. The advantages of a Class D amplifier are high efficiency, linearity and ruggedness, since power is ideally dissipated only during the switching transitions.

These amplifiers are readily applicable for FM modulation, after harmonic filtering. The analog gain is obtained by pulse-width modulation of the input switching signal, and demodulation of the output with suitable filters. Linearity is required only from the modulator, which is easy to achieve at small signal levels. The high speed voltage controlled one shot MC10198 should be ideal for a linear pulse-width modulator. By properly adjusting its operating point, low level AM or suppressed carrier double sideband signals can be generated.

GENERAL

All MOSFETs can in theory have a positive temperature coefficient on the gate threshold voltage. This means that the gate threshold voltage increases with temperature, trying to “turn the device off.” In addition the gm will decrease, which also helps in preventing the thermal runaway, which is commonly a problem with bipolars. The coefficient of the gate threshold voltage is also a function of the drain current. Normally the coefficient is negative at low current levels, and turns positive at higher currents. The turnaround point, which can be controlled by doping the other fabrication steps, must be at a current level not to exceed the maximum dissipation rating, taking the derating factor into account. Thus, the power MOS devices can be easily biased to Class A, without fear of a thermal runaway.

CONCLUSION

From the above we must conclude that it is doubtful the power FET ever will replace the bipolar transistor in all areas of communications equipment. It will have its applications in low and medium power VHF and UHF amplifiers, eliminating the need for internal matching, and up to medium power low band and VHF SSB, where the high order IMD is beginning to be more and more in emphasis due to the crowded frequency spectrums. The author’s personal opinion is that the power FET is the most feasible device for the amplitude compandored sideband (ACSB) applications, proposed for future use in land mobile communications. The system principle requires extreme linearity in the amplifying stages, which in the past has only been achieved with Class A operation. The power FET also opens new applications for high efficiency switching mode power amplifiers, which have not been possible in the past for reasons described earlier. The possible upper frequency limit would be dictated by the physical lay-out of the system.
Figure 8. An Experimental Three Stage, One Kilowatt Class D Amplifier. The unit operates up to 10 MHz yielding an efficiency of 85 percent. The power gain is 30 dB.
Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer’s technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and \( ^{2} \) are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanner’s Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.