AN1526

RF Power Device Impedances: Practical Considerations

Prepared by: **Alan Wood and Bob Davidson**
Motorola Semiconductor Products Sector

ABSTRACT

The definition of large–signal series equivalent input and output device impedances for RF power transistors is explained, together with the techniques for measuring these parameters. How these parameters change under varying load and bias conditions is examined, and the impact of these variations is demonstrated in a practical broadband test fixture design.

INTRODUCTION

Many first time RF power designers, brought up on a diet of small–signal s–parameters, previously used for solving small signal text book problems, assume these same techniques are applicable to bipolar class–C and class–AB power amplifier design. They consider the best match is achieved by a simultaneous conjugate match of the input and output. However, power amplifiers provide higher power gain and better efficiency at the rated output power if the output is purposely mismatched. An added benefit of doing this is potentially unstable devices, conjugately matched, can be operated stably under these more optimum mismatched conditions.

More knowledgeable designers, familiar with large–signal impedances, naively assume the published impedances are independent of operating point. They forever wonder why, although they have designed their impedance transformation networks to match the device "data book impedances," they have to "tweak" the circuit for optimum performance. This is the basis for much of the black magic that surrounds RF power amplifier design, but the reality is the circuit designer is plagued with a paucity of good design data, and a lack of adequate tools to make the initial design "foolproof." This paper intends to enlighten these engineers to the true meaning of large–signal series equivalent device impedances. We will also show that the output impedance is, for the most part, under the control of the circuit designer, and the input device impedance can be expected to change depending upon the designers choice of output matching (or, in some cases, intentional mismatching).

DEFINITIONS

Small–signal s–parameters have gained a great deal of acceptance in low power linear amplifier design. Unfortunately, progress in large–signal power amplifier design has been less substantial. Techniques have been published over the years, e.g. large–signal s–parameters; load–pull; and stability analysis using small–signal s–parameters, but they have not gained wide spread acceptance for a number of reasons, including the degree of applicability and the ease and accuracy of the measurements. The universal starting point for RF power amplifier design remains the published large–signal impedances. These techniques are discussed briefly below, outlining their advantages and disadvantages.

Small–Signal S–Parameters

Small–signal RF designers are very familiar with the classic s–parameter [1] characterization and design methods for small–signal linear devices. Data is usually available at multiple collector bias voltage and current conditions over a wide range of frequencies. The ease of making these measurements accurately with modern network analyzers has done a great deal for systemizing small–signal RF amplifier design. The availability of software for analyzing and optimizing the performance of broadband amplifiers and establishing their stable operation has further improved the design methodology. However, when the designer is asked to step into the high power RF design world, he is immediately confronted with several possible device characterization methods. First of all, let's understand the term "high power." As used in this paper, we are talking about RF power amplifier devices with output powers from roughly one watt to several hundred watts. At these power levels, the small–signal s–parameters lose their usefulness in determining appropriate source and load reflection coefficients, to say nothing of the familiar gain and stability circles or non–unilateral issues. This is because high power class–C RF amplifiers are VERY non–linear. The industry standard s–parameters are valid only for devices operated in small–signal linear conditions. These parameters have very limited use in high power applications. One exception is presented by Frost, [2] in using the "large–signal s–parameters" as an aid in the stability analysis process. Hejhall, [3] also demonstrates the use of small–signal s–parameters for stability analysis in FET power amplifier design and shows their utility when large–signal impedances are unavailable.

Large–Signal S–Parameters

The availability of network analyzers and the subsequent ease of measuring small–signal s–parameters has led to a characterization technique referred to in the literature as "large–signal s–parameters." Successful measurement and usage of these parameters has been reported [4]–[12]. However, the authors are not aware of these parameters being used successfully above a few watts of output power. Measurement of these parameters is usually accomplished by driving the device from a 50 ohm source to achieve a collector or drain current comparable to that expected in actual operation.

MOTOROLA

Devices with output power ratings above a few watts have input reflection coefficient magnitudes very close to one, requiring drive levels far beyond the capability of a standard network analyzer to merely turn the device on, if operated in class–C. This restriction can be alleviated to some extent, by providing a degree of impedance matching between the network analyzer ports and the device, and de–embedding the device from the impedance transforming network. There is also a question of the validity of the S22 and S12 measurements for class–C design. If the device is biased off, as is normally the case in class–C, the measurements of these two parameters will be in err. Ideally, the transistor should be operating with drive applied to the input when making these measurements. The test signal can then be applied to the output port and the reverse gain and output reflection coefficient measured with the device at a normal operating bias. This method is described in more detail by Mazumder [8]. Harmonic loading of the device is a factor not addressed by most large–signal s–parameter proponents but plays a significant part in the non–linear operation of RF power amplifiers.

In addition, these measurements require EXTREME caution. Making a direct connection of a network analyzer to a potentially unstable 100$^+$ watt device could be very hazardous to the network analyzer. Custom built test sets and measurement systems are almost always required. Further, this type of characterization gives the designer no information as to how other parameters, such as efficiency, behave with fundamental load impedance variations.

Load–Pull

Another characterization technique is referred to in the literature as "load–pull" [16]–[24]. This technique results in the graphical presentation of a performance parameter such as gain, efficiency or IMD, versus a source or load impedance. Although the technique has been known for some time, the widespread availability of desktop computers and automatic tuning systems is just now making this method more attractive, particularly for higher power devices. The characterization process is conceptually quite simple. A variety of load impedances are presented to the device as shown in Figure 16. The performance of the device is measured at each one of these points, and fed into a surface generating program. (See the appendix for further information). Figure 1 shows an example of how the gain of the 15 watt MRF873 varies at 870 MHz with various fundamental frequency load impedances. Figure 2 shows how the collector efficiency of this device varies under the same conditions. The influence of output load impedance on input impedance, due to finite reverse transfer, is illustrated by the input return loss surface in Figure 3. These surface plots are converted to contour plots in Figures 4–15. Now the designer can easily see areas of the reflection coefficient plane where the matching network should not be centered, due to a high degree of variability in a particular performance parameter. A method has been proposed by Stancliff and Poulin [25] to examine the load–pull performance of a device by varying not only the fundamental frequency impedance presented to the device, but also the second harmonic impedance as well. This technique can provide the designer with extremely useful information about the device's behavior.

These benefits do not come without some labor. In general, load–pull data is usable only at the operating conditions at which it is measured. As can be seen in Figure 16, a large set of load impedance points must be presented to the device output, in order to construct the power gain and efficiency contours. Changes in bias voltage or output power require the re–taking of data over the same range of load impedance conditions. Without proper equipment this type of characterization is very tedious, time consuming, and prone to errors. With the advent of automated tuners measurement of the data is not as time intensive as some of the earlier methods, and computer software can be used to manipulate the data and fit the contours. For power devices it does require a test fixture with some degree of impedance matching, and the matching networks must be characterized so that the device impedances can be de–embedded.

If data is available over the whole band, the gain response with frequency can be optimized for flatness and best efficiency, by selecting a low frequency load line impedance on a constant gain circle that compensates for the inherently higher gain of the transistor at lower frequency. Broadband solutions from network design programs i.e. SuperCompact™ and Touchstone™ can be evaluated to assess how much they have comprised gain and efficiency throughout the band in arriving at a broadband match.

Large–Signal Series Equivalent Impedances

The classic technique of high power device characterization used by Motorola is that of large–signal series equivalent input and output impedances as presented by Hejhall [13]. Almost every RF power device in Motorola's RF Device Data Book has a section identifying the device's large–signal series equivalent input and output impedances. Most often, the device output impedance is referred to as "the complex conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency." That is certainly a statement requiring some careful thought, especially since the term "output impedance" is somewhat misleading. The designer new to high power devices should be aware that this so called "output impedance" has no connection with the S_{22} small–signal measurement. Rather, as described in [13], it is the conjugate of the LOAD impedance at the fundamental operating frequency which allowed the transistor to "function properly." The designer should also be aware that the characterizations on a device's data sheet are valid for some very specific conditions of frequency, supply voltage, input or output power, bias levels, harmonic loading and even flange temperature. The output impedance published in the data sheet is usually the conjugate of the LOAD impedance that provides maximum gain at a given output power. Suppose the designer is interested in maximum efficiency, not maximum gain. As seen in the load–pull contours the fundamental frequency load impedance producing maximum efficiency does not coincide with the maximum gain impedance. It is up to the device designer to choose which impedance gets published. One is just as valid as the other. However, quite frankly, gain is what sells devices. Likewise, Figures 7, 11 and 15 show how the input return loss, and thus the device input impedance, is also a function of the load impedance. The input impedance for higher power

devices is a much stronger function of load impedance than shown for this small device.

Device impedances published by vendors of RF power transistors should only be used as an approximation for a first cut circuit design. In a broadband amplifier design it is often difficult to obtain a good match over the full frequency range and in certain circumstances the input or output is deliberately mismatched to compensate for the gain increase at lower frequencies to provide a level gain response. Good design would opt for a load–line where the lower gain corresponds to a higher efficiency operating point.

MRF873 DEVICE IMPEDANCE COMPARISON FOR DIFFERENT MODES OF OPERATION

Device characterization techniques are not the only difference in the way a high power RF device is specified. Many devices are specified and characterized for class–C or –AB operation. Common questions when using a device differently from the way it is characterized in its data sheet are: "What will the gain be?", "What are the impedances?" In general, power gain is highest when the device is operated in class–A and slightly lower when the device is operated in class–AB. Power gain is lowest when operating in class–C decreasing as more reverse bias is applied to the base and the transistor conduction angle decreases. The designer should beware, a transistor designed to be rugged, i.e. capable of withstanding a specified output mismatch under class–C conditions, will be LESS RUGGED with forward bias applied to the base. Device impedances depend not only on the internal structure of the device, but also how that device is operated. For small–signal operation with the device biased in class–A, the optimum device input and output impedances, for a stable device, are the simultaneous conjugately matched impedances which can be derived from the s–parameters.

For power operation the optimum output impedance is a function of the output power, the collector bias voltage and the output reactance of the transistor. The required peak output power and the collector bias voltage determine the operating load line. The output reactance of the device under these conditions is conjugately matched to achieve maximum power transfer, although this condition may be modified, at the expense of gain, to attain higher efficiency.

The load line resistance is given approximately by:

$$R_L = \frac{(V_{CC} - V_{CE(sat)RF})^2}{2 * P_{out}} \tag{1}$$

where V_{CC} is the collector supply voltage,
P_{out} is the required peak power,

and $V_{CE(sat)RF}$ is the collector–emitter saturation voltage under the frequency of operation. The value of this parameter is particularly difficult to measure, but the normal range is 1.0 to 2.5 Volts depending on the geometry, epitaxial doping and thickness. A good approximate value for 12.5 Volt devices is 1.5 Volts and for 24 Volt transistors is 2 Volts.

The load line resistance is the optimum load impedance for the internal collector node of the transistor, neglecting the junction and parasitic device capacitance. These are in parallel with the load line resistance. For transistors, operating at VHF, and above the internal collector lead inductance of the package becomes significant, and is in series with the previously defined parallel R_L, C_{obo} network. For the CS–12 package the internal collector lead series inductance can be represented by a 0.65 nH lumped inductor. Some devices have internal collector matching, transforming the internal load line impedance to higher value for ease of broadband matching.

Comparison of the impedance data taken by small–signal methods, assuming a simultaneous conjugate match, and large–signal measurements, shows dramatic shifts in input impedance (see Table 1). More subtle, but measurable differences, can be seen in the change in input impedance between class–C and class–AB data. The small–signal s–parameter data is given in Table 2 below for a collector bias current of both 50 mA and 2 A.

Table 1. Comparison of Input Impedance for Different Operating Modes

Frequency (MHz)	Simultaneous Conjugate Match (I_{CQ} = 50 mA)	Class–AB (I_{CQ} = 50 mA)	Class–C
806	0.478 – j3.19	1.33 + j3.34	1.10 + j3.26
838	0.503 – j3.41	1.43 + j3.41	1.19 + j3.24
870	0.568 – j3.48	1.50 + j3.32	1.24 + j3.34

Table 2. Small–Signal S–Parameter Data for the MRF873 at V_{CC} = 12.5 Vdc

Frequency (MHz)	I_C	S_{11}		S_{12}		S_{21}		S_{22}	
		$\|S_{11}\|$	$\angle \phi$	$\|S_{12}\|$	$\angle \phi$	$\|S_{21}\|$	$\angle \phi$	$\|S_{22}\|$	$\angle \phi$
806	50 mA	0.963	172.8	0.006	7.72	0.437	– 4.95	0.910	– 163.5
	2 A	0.877	170.9	0.024	27.9	1.567	12.7	0.697	– 174.5
838	50 mA	0.961	172.4	0.005	4.12	0.436	– 11.0	0.928	– 164.5
	2 A	0.858	172.7	0.022	17.5	1.639	– 3.30	0.723	– 169.9
870	50 mA	0.958	172.3	0.004	8.35	0.435	– 17.7	0.948	– 165.4
	2 A	0.861	175.3	0.018	6.31	1.592	– 21.7	0.789	– 166.8

Table 3. MRF873 Impedance Data Computed from S–Parameters (I_C = 50 mA)

Freq. (MHz)	Input Z [S_{11}]	I/P Simul. Conjugate. Match	Output Impedance	O/P Simul. Conjugate Match	Data Book Z_{OL}	Optimum O/P Impedance From Load Pull	K	B1
806	0.95 + j3.15	0.48 – j3.19	2.41 – j7.24	1.19 + j7.15	2.93 – j1.39	3.60 +j1.26	1.62	0.336
838	1.00 + j3.31	0.50 – j3.41	1.90 – j6.79	0.94 + j6.61	2.92 – j1.10	3.60 +j1.02	1.61	0.270
870	1.07 + j3.37	0.57 – j3.48	1.35 – j6.41	0.71 + j6.27	2.92 – j0.81	3.39 + j0.75	1.71	0.197

Table 4. MRF873 Impedance Data Computed from S–Parameters (I_C = 2 A)

Freq. (MHz)	Input Z [S_{11}]	I/P Simul. Conjugate. Match	Output Impedance	O/P Simul. Conjugate Match	Data Book Z_{OL}	Optimum O/P Impedance From Load Pull	K	B1
806	3.29 + j3.95	1.13 – j2.98	8.94 – j2.31	2.86 + j5.52	2.93 – j1.39	3.60 +j1.26	1.145	0.941
838	3.83 + j3.18	1.06 – j2.90	8.09 – j4.32	2.10 + j5.14	2.92 – j1.10	3.60 +j1.02	1.12	0.871
870	3.74 + j2.02	1.02 – j2.86	5.99 – j5.72	1.57 +j4.69	2.92 – j0.81	3.39 + j0.75	1.12	0.693

Since class–C circuits are biased at cut–off and class–AB at low quiescent current compared to the collector current at peak output power there is a question at which bias point to take the s–parameters.

Below is a comparison of the device impedances computed from the s–parameters at a typical bias current for class–AB operation and the same measurements at a collector current corresponding to operation of the device at rated output power under class–C conditions.

This data shows a large shift in the impedances computed from the s–parameter data introduced by changing the bias point. For this particular transistor, it indicates the simultaneous conjugate match impedances, taken at a collector current more in line with the current under class–C conditions, are a better match to the conjugate of the class–C impedances. Comparison of the output simultaneous conjugate match impedance with the relatively higher optimum load line impedance from the load–pull measurements, illustrates how the load line has been shifted to increase the efficiency of the amplifier. A rough calculation of the collector efficiency from $(Re(Z_{opt})/[Re(Z_{opt}) + Re(ZM1)])$ gives a value of 68% at 870 MHz, very close to the actual value of 70% from the efficiency contours with the same load–line. Note maximum power transfer cannot usually be achieved with a simultaneous conjugate match because of non–linear current limiting characteristics of the device.

CURRENT METHODS OF ENSURING CONSISTENT DEVICE IMPEDANCES

Users of RF power transistors have two main concerns with regard to the long term consistency of the device, minimum gain requirements and consistent impedances. Most of the recent devices characterized for the land mobile environment utilize a broadband fixture to demonstrate performance over a range of frequencies. The recently introduced MRF650 goes a step further and specifies gain, efficiency and input return loss at three frequencies of operation in a specified test fixture. Motorola has found over the years that this is the most cost effective way of producing RF power devices with minimum variability. Of course, new testing and characterization techniques are constantly being evaluated. The engineer unfamiliar with RF power devices

will probably ask, "If the fixture is used to produce a consistent device, what produced the fixture?" The answer lies in the device development process.

During the development of an RF power transistor, sample devices are typically evaluated in narrowband tuneable fixtures. During this evaluation period, the device designer is balancing a multitude of performance parameters with customer and manufacturing requirements. By the end of the evaluation period, devices from quite a wide distribution will have been constructed. These devices are then used to design a broadband fixture to be used in characterization and factory testing of the production part. A typical broadband fixture and circuit schematic are shown in Figures 20 and 21 for the MRF873 RF power transistor. Broadband performance for this fixture is shown in Figure 25. Specifications for the device are based on this fixture and the devices that defined it. A portion of these evaluation devices are locked away and referred to as "master engineering correlation units." Motorola's philosophy is that in the event of a damaged or irreplaceable fixture, these master devices are sufficient to duplicate the fixture. To be sure, there is considerable data taken on the original fixture. This data is not limited to RF performance but also includes such information as broadband source and load impedance sweeps. The engineer new to RF power design must understand that the impedances presented in the data sheet ARE NOT the impedances of the broadband fixture.

Data Book Impedances

Data book impedances are normally taken at the rated output power and nominal supply voltage. The transistor is operated in a test fixture with a range of tuning either by on–board trimming capacitors or external tuners or a combination of both methods. The impedances seen in the data sheet represent the average of several devices placed in a narrowband fixture and tuned, usually for maximum gain, at a specific output power, supply voltage and frequency with reflected power minimized to at least –25 dB input return loss. The device is removed and the SOURCE and LOAD impedances at Fc are measured with the reference plane at the device package edge. A piece of information NOT specified on Motorola data sheets (or any other vendor's data sheet known to the authors) is the impedances at the

harmonic frequencies presented to the device. In most cases, it is the first shunt capacitance combined with the device package series inductance that determines the second harmonic impedance present at the INTERNAL collector–emitter terminals. The designer should simply be aware that it is possible to have a perfect match at the fundamental frequency and NOT get the published performance due to improper harmonic terminating impedances.

A further point of clarification is the measurement technique for these very low impedances. Several techniques exist for the measurement of the source and load impedances presented to a device. The simplest approach is to construct an impedance measuring probe similar to those shown in Figures 17–19. These probes are nothing more than a blank device package appropriate for the fixture being used, with a short piece of small semi–rigid 50 ohm coax carefully soldered in place. The most convenient method of calibration is to first perform a full one–port calibration on the network analyzer using a 3.5 mm calibration kit. Then, with the probe clamped into the tuned test fixture and a piece of copper foil slipped under the probe's center tab, use a port extension to reset the phase angle at the frequency of interest to 180 degrees. This technique is valid for 1/2″ CQ packages through 520 MHz. Square packages such as the CS–12 can be used up to 1 GHz. An error is present due to the discontinuity between the end of the semi–rigid coax and the package edge. This discontinuity has been de–embedded and found to be negligible.

Break–Apart Test Fixture

A technique which avoids these discontinuities involves a fixture which can be "broken apart" at the reference planes. Figure 22 shows the construction of the break–apart test fixture. After tuning the circuit for the desired performance the test fixture is broken apart, the bridge on which the device sits removed, and co–axial connectors installed at the reference planes (Figure 23). The impedances presented to the device can then be measured using the network analyzer calibrated with a standard 'N' type calibration kit, and a port extension applied to rotate out to the reference plane.

In the off–line impedance measurement techniques described above, the break–apart test fixture offers the advantages of improved repeatability and more consistent measurement plane location. This is at the expense of more time intensive measurements, since at each frequency point, the fixture has to be partially disassembled and connectors installed before impedances can be measured. The break–apart test fixture really comes into its own when used for in–line impedance measurements. Each half of the fixture can be characterized as a two port using a network analyzer, and with a knowledge of the impedances presented externally to the test fixture, the device impedances can be de–embedded [26]–[30]. The test fixture provides the all important "close in" match and a measure of broadband performance, while the external tuners provide the fine tuning at the measurement frequencies within the operating band. The test fixture also provides biasing for the transistor at current levels higher than can normally be accommodated by external bias tees, and if correctly bypassed, improves the stability under mismatch conditions.

Automated Tuners

Automated tuners offer a number of advantages. If used wisely, they can provide in–line impedance measurement capability, and allow rapid characterization of a device under load–pull conditions. In–line measurement of device impedances makes it practical to measure a sufficient number of devices to establish impedance distributions for a particular device type. Currently available systems are, however, still too slow to use in a production environment for 100% testing of RF transistors. Load–pull characterization can be performed under custom conditions enabling an amplifier designer to start the matching network synthesis with impedance data representative of the final operating conditions.

Automated tuners need to be coupled with some type of impedance matching test fixturing for three very important reasons. a) The impedance transformation range is normally limited to 10:1 precluding their use with most power transistors that have relatively low input impedances outside this range. b) Optimum performance of a power amplifier requires careful attention to the harmonic loading, which in many cases requires shunt capacitance close to the package. The low input/output impedances also require low loss return paths for the circulating ground currents. c) Bias networks can be designed on the test fixture to minimize the potential for instability necessary for correct operation of automated tuner search algorithms.

Measurement Accuracy Factors

There is some tolerance in the package dimensions which dictates that the test fixture be designed with some mechanical tolerance to allow devices to be tested at the maximum extremes of the device width and height over the seating plane. The contact of the leads to the test fixture pads is therefore variable contributing additional series inductance to the input, output and ground leads. This results in more inductive device impedances than expected if careful steps are not taken to minimize this error.

Absolute Accuracy of Measurement Instrument, Network Analyzer

Great improvements have been made in network analyzer measurement accuracy over the last ten years [32]–[37]. Not too many years ago device impedances were routinely measured with vector voltmeters, using only a single correction term for the frequency response of the couplers. Now, for 1 port measurements, three term error correction is the norm, correcting for directivity, source mismatch and frequency response. The network analyzer does still introduce a degree of measurement uncertainty proportional to the magnitude of the reflection co–efficient. This is more of a problem with higher power devices where the real part of the impedances can be below 1 ohm. The reader is referred to the manufacturers operating manuals for the maximum possible magnitude of the error. In the worst case, for a transistor with a 1 ohm real part of the impedance, the error can be as large as ± 1 ohm.
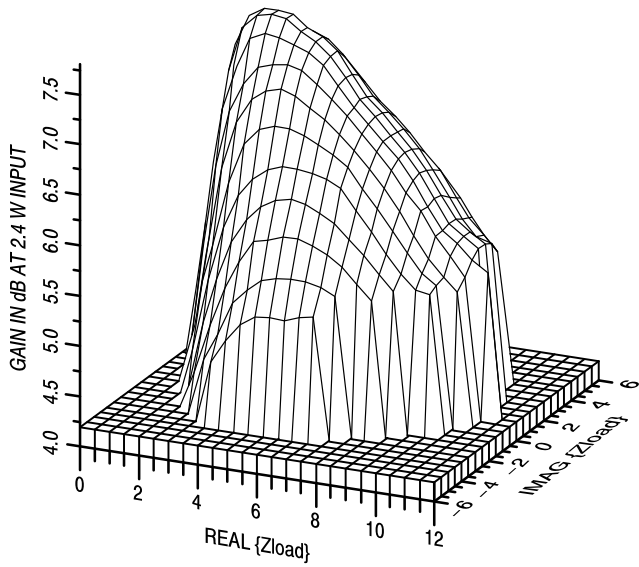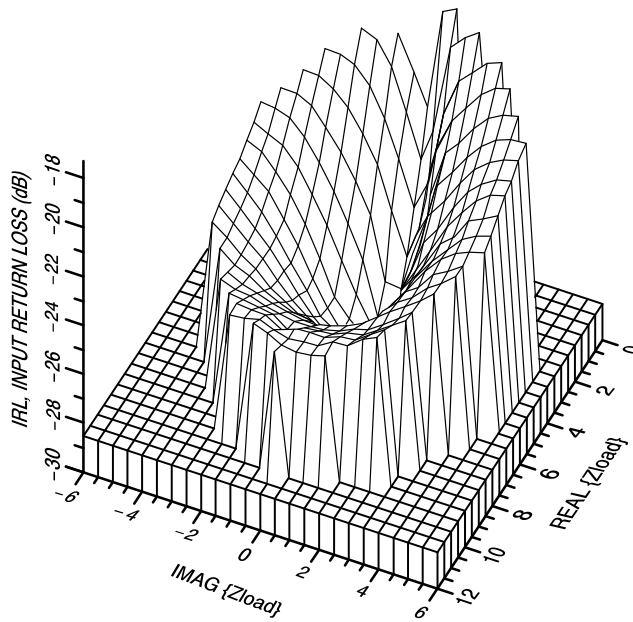
870 MHz, Class–C, V_{CE} = 12.5 VDC, P_{in} = 2.4 Watts

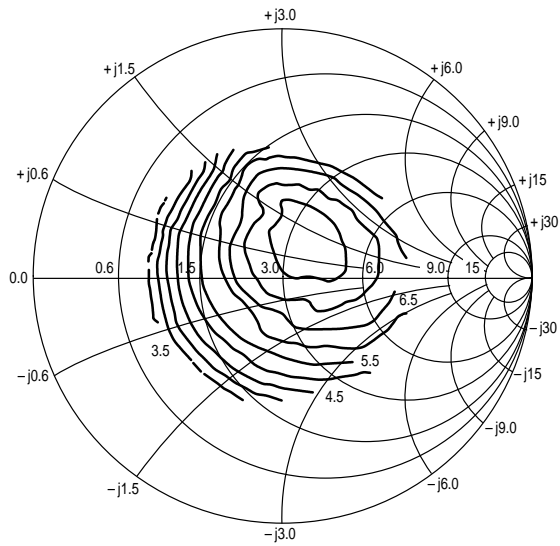**Figure 1. MRF873 Gain Surface vs
Fundamental Load Impedance**
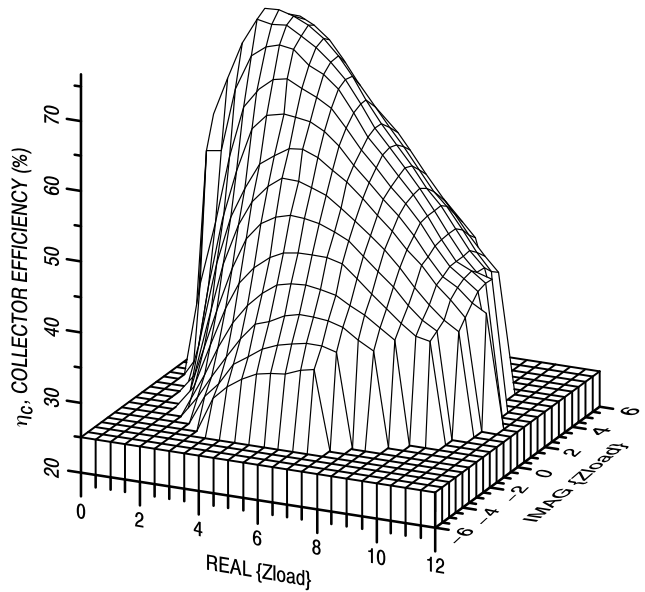
870 MHz, Class–C, V_{CE} = 12.5 VDC, P_{in} = 2.4 Watts

**Figure 2. MRF873 Efficiency Surface vs
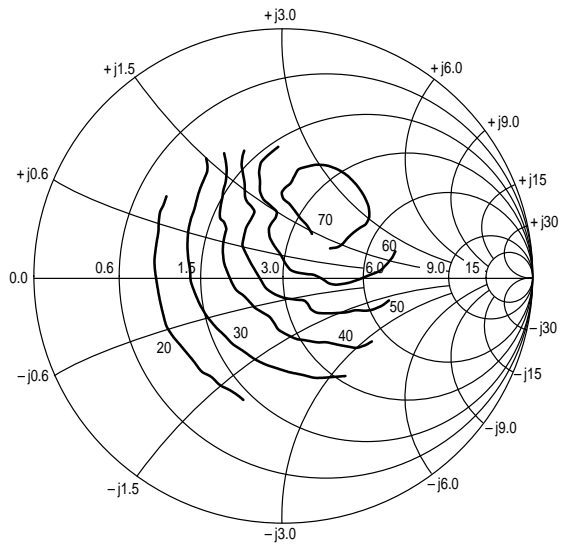Fundamental Load Impedance**

870 MHz, Class–C, V_{CE} = 12.5 VDC, P_{in} = 2.4 Watts

**Figure 3. MRF873 Return Loss Surface vs
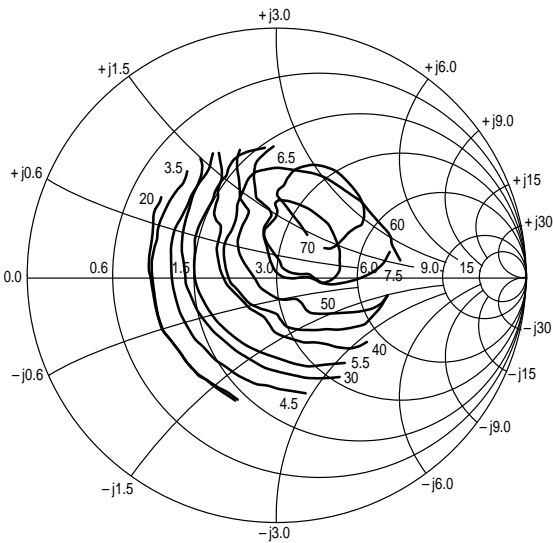Fundamental Load Impedance**

Load Impedance Chart Z0 = 3.0 Ohms
806 MHz, Class–C, V_{CE} = 12.5 VDC, P_{in} = 2.4 Watts

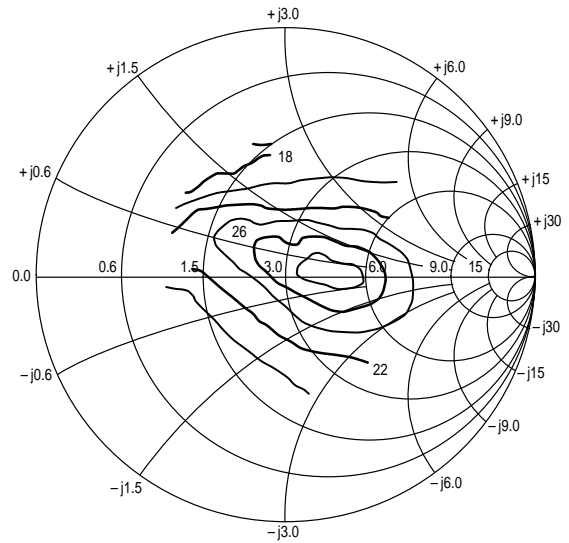**Figure 4. MRF873 Constant Gain Contours**

Load Impedance Chart Z0 = 3.0 Ohms
806 MHz, Class–C, V_{CE} = 12.5 VDC, P_{in} = 2.4 Watts

Figure 5. MRF873 Constant Efficiency Contours

Load Impedance Chart Z0 = 3.0 Ohms
806 MHz, Class–C, V_{CE} = 12.5 VDC, P_{in} = 2.4 Watts

**Figure 6. MRF873 Combined Gain
and Efficiency Contours**
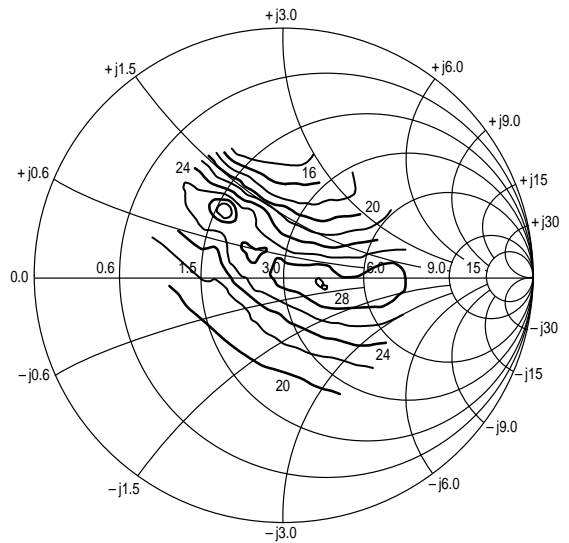
Load Impedance Chart Z0 = 3.0 Ohms
806 MHz, Class–C, V_{CE} = 12.5 VDC, P_{in} = 2.4 Watts

**Figure 7. MRF873 Constant Input
Return Loss Contours**
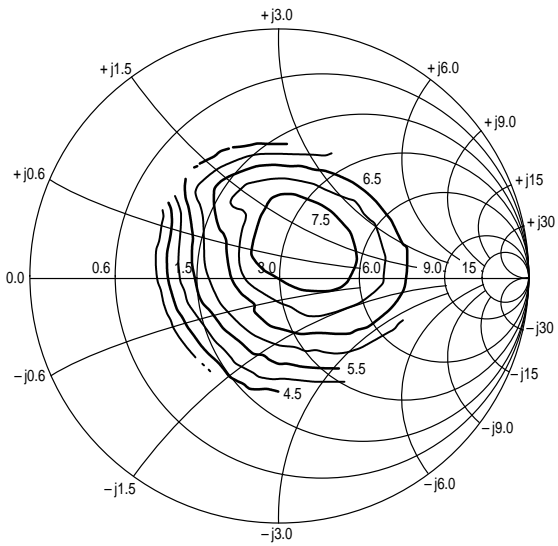
Load Impedance Chart Z0 = 3.0 Ohms
838 MHz, Class–C, V_{CE} = 12.5 VDC, P_{in} = 2.4 Watts

Figure 8. MRF873 Constant Gain Contours
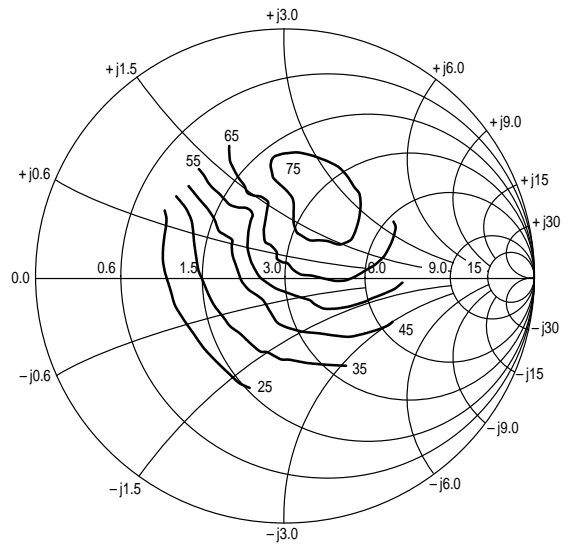
Load Impedance Chart Z0 = 3.0 Ohms
838 MHz, Class–C, V_{CE} = 12.5 VDC, P_{in} = 2.4 Watts

Figure 9. MRF873 Constant Efficiency Contours
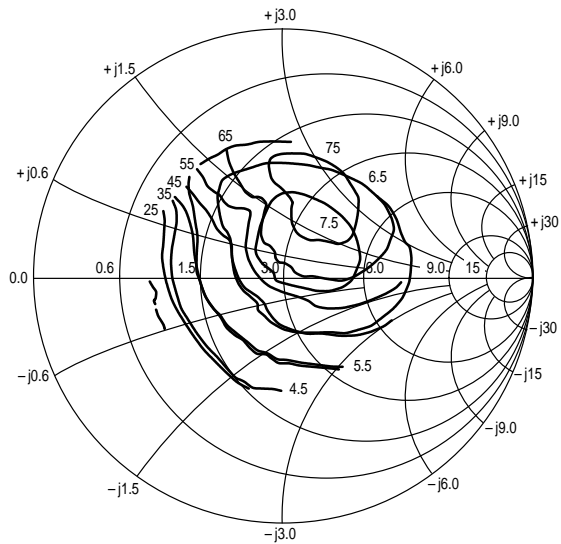
Load Impedance Chart Z0 = 3.0 Ohms
838 MHz, Class–C, V_{CE} = 12.5 VDC, P_{in} = 2.4 Watts

**Figure 10. MRF873 Combined Gain
and Efficiency Contours**
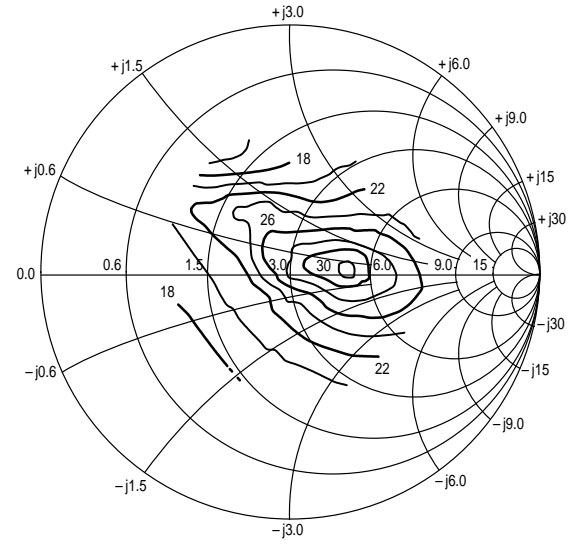
Load Impedance Chart Z0 = 3.0 Ohms
838 MHz, Class–C, V_{CE} = 12.5 VDC, P_{in} = 2.4 Watts

**Figure 11. MRF873 Constant Input
Return Loss Contours**
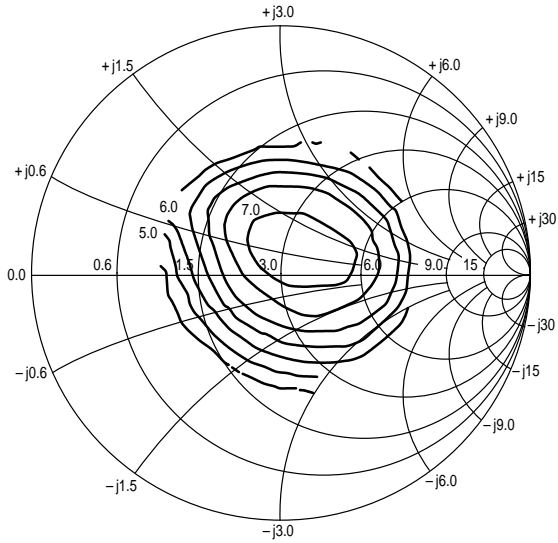
Load Impedance Chart Z0 = 3.0 Ohms
870 MHz, Class–C, V_{CE} = 12.5 VDC, P_{in} = 2.4 Watts

Figure 12. MRF873 Constant Gain Contours
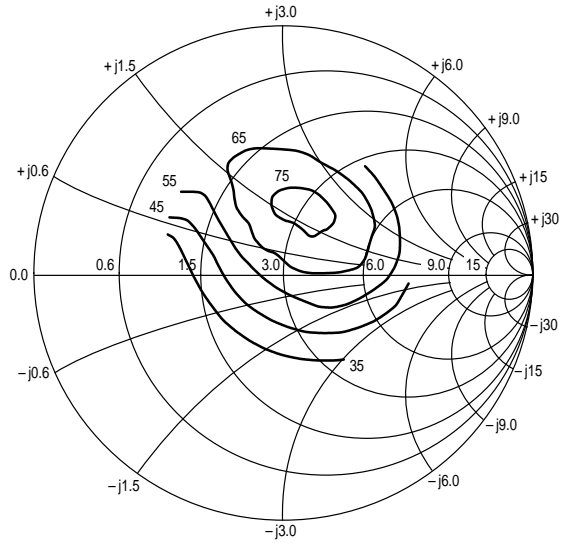
Load Impedance Chart Z0 = 3.0 Ohms
870 MHz, Class–C, V_{CE} = 12.5 VDC, P_{in} = 2.4 Watts

Figure 13. MRF873 Constant Efficiency Contours
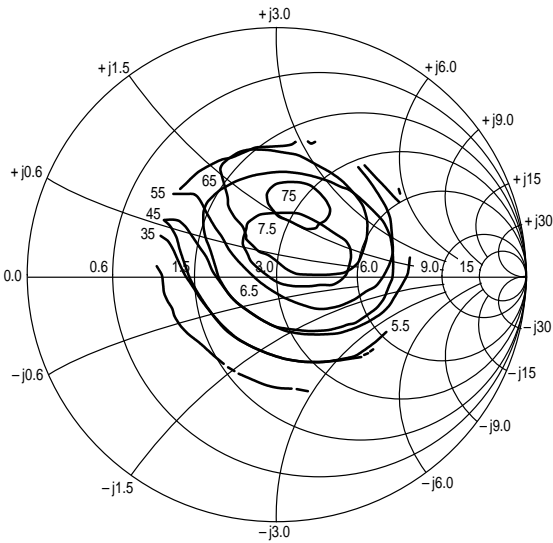
Load Impedance Chart Z0 = 3.0 Ohms
870 MHz, Class–C, V_{CE} = 12.5 VDC, P_{in} = 2.4 Watts

**Figure 14. MRF873 Combined Gain
and Efficiency Contours**

Load Impedance Chart Z0 = 3.0 Ohms
870 MHz, Class–C, V_{CE} = 12.5 VDC, P_{in} = 2.4 Watts

**Figure 15. MRF873 Constant Input
Return Loss Contours**
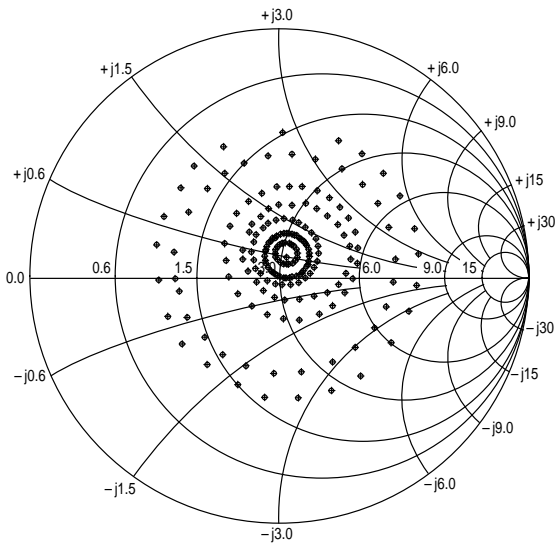
Chart Z0 = 3.0 Ohms

Figure 16. Load–Pull Impedances Presented to MRF873 at 870 MHz

MSUB		ER = 1	H = 2000	T = 6	RHO = 1	RGH = 0			
CPW		1	2	W = 205	G = 45	L = 160			
MSUB		ER = 9.6	H = 60	T = 6	RHO = 1	RGH = 0			
CPW		2	3	W = 235	G = 20	L = 116			
CAP		3	0	C = 0.29					
WIRE		3	4	D = 15	L = 40				
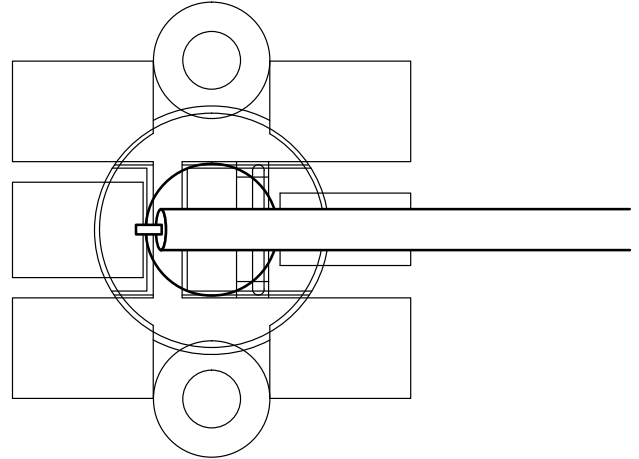
Figure 17. Drawing of 1/2″ CQ Package Impedance Measurement Probe Including De–Embedding Circuit Model

Figure 18. Photograph of CS–12 Impedance Measurement Probe

Figure 19. Photograph of 1/2″ CQ Impedance Measurement Probe
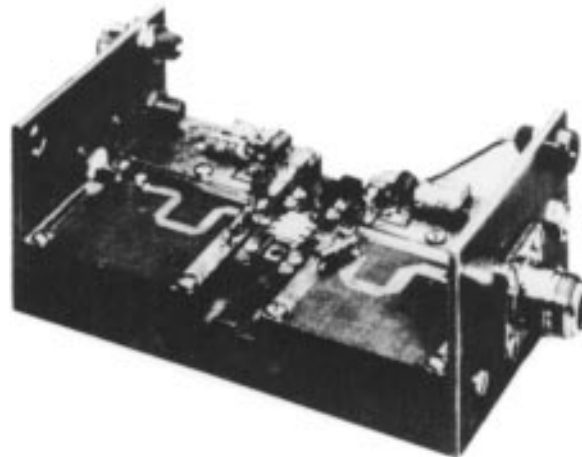
Figure 20. Photograph of MRF873 Broadband Production Test Fixture
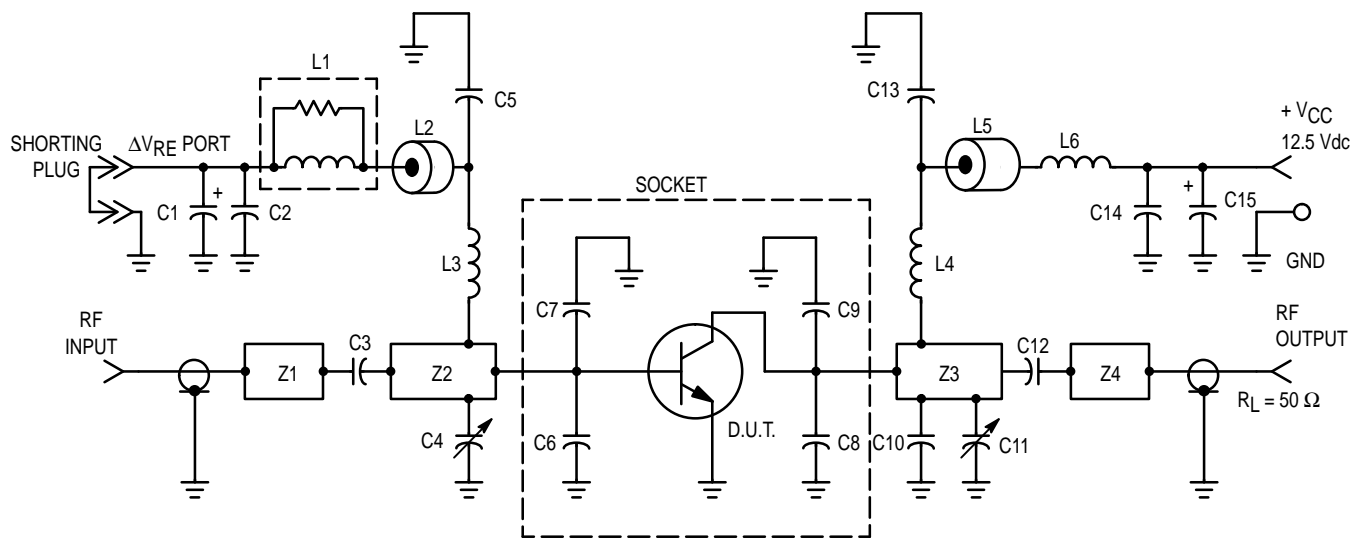
C1, C15 — 10 μF, 25 V Tantalum
C2, C14 — 1000 pF, 350 V, Unelco
C3, C12 — 43 pF, 100 Mil, ATC Chip Capacitor
C5, C13 — 91 pF, Mini–Unelco
C4, C11 — 0.8 – 8 pF, Johansen Gigatrim 7290 Variable
C6 — 16 pF, Mini–Underwood
C7, C8, C9 — 12 pF, Mini–Underwood
C10 — 10 pF, Mini–Underwood

NOTE: C11 ≈ 0.4″ down Z3 from socket edge.

L1 — 13 Turn, #20 AWG Around 10 Ω, 1/2 W, Resistor
L2, L5 — Ferroxcube Bead #56–590–85–38
L3, L4 — 4 Turns, #20 AWG Choke ID 0.2″
L6 — 6 Turns, #20 AWG Choke ID 0.2″
Z1, Z4 — 50 Ohm Microstrip
Z2 — 36 Ohm Microstrip $\lambda/4$ @ 838 MHz
Z3 — 26 Ohm Microstrip $\lambda/4$ @ 838 MHz

Board Material — 0.032″ Glass Teflon 2 oz. Copper Clad ε_r = 2.55

Figure 21. MRF873 Boardband Production Test Fixture Schematic
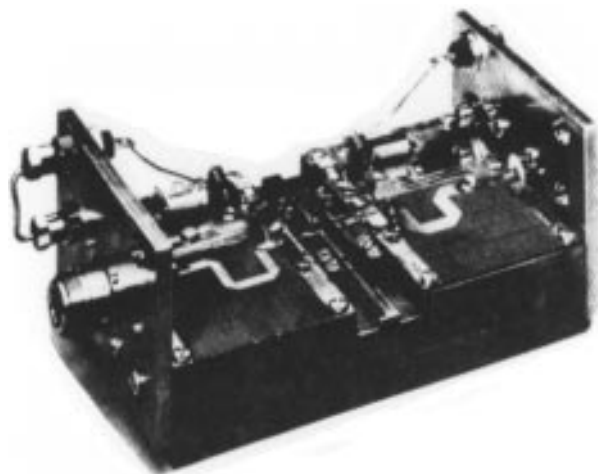
**Figure 22. Photograph of Break–Apart Test Fixture —
Fully Assembled**
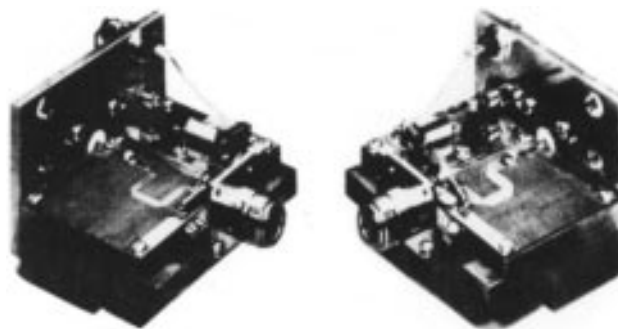
**Figure 23. Photograph of Break–Apart Test Fixture —
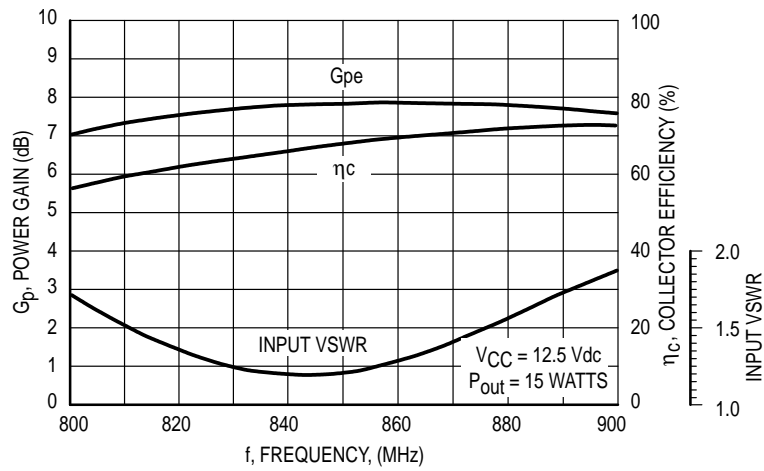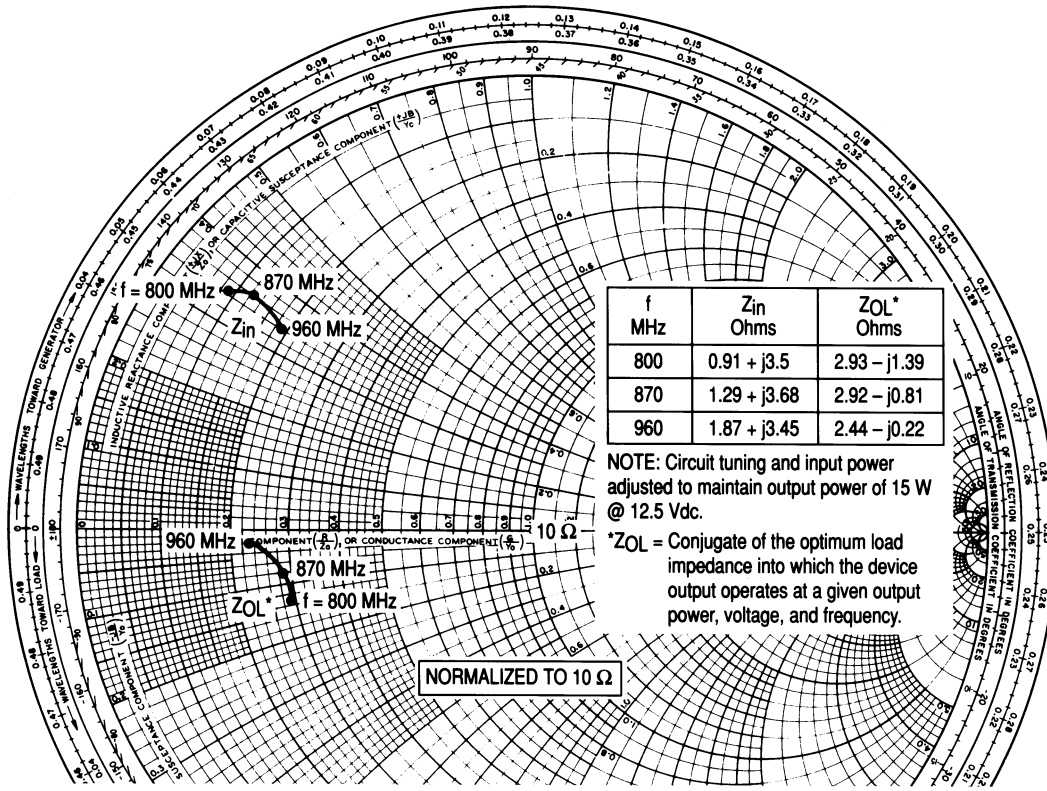Setup for Impedance Measurements**
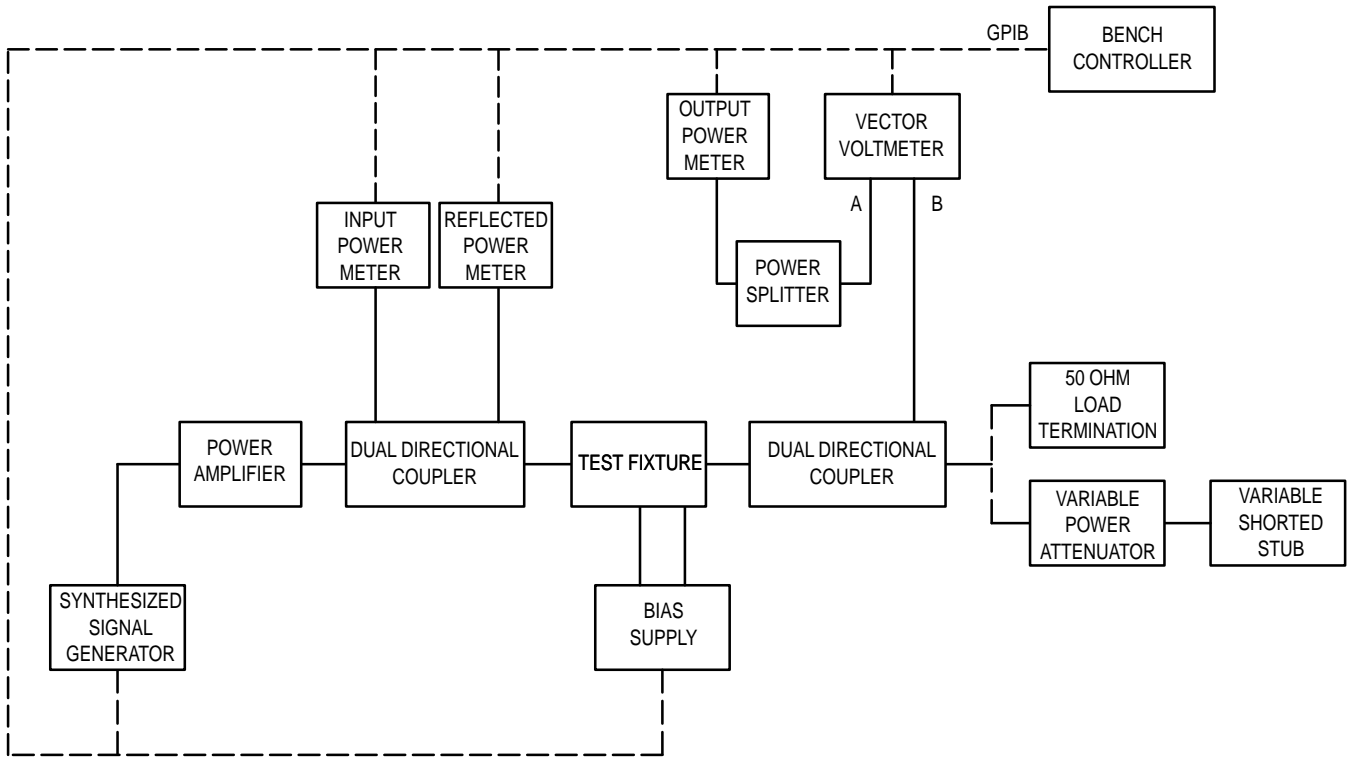
Figure 24. Load–Pull Test Setup

V_{CE} = 12.5 VDC, P_{out} = 15 Watts

**Figure 25. Broadband Performance of
MRF873 Production Test Fixture**

f MHz	Z$_{in}$ Ohms	Z$_{OL}$* Ohms
800	0.91 + j3.5	2.93 − j1.39
870	1.29 + j3.68	2.92 − j0.81
960	1.87 + j3.45	2.44 − j0.22

NOTE: Circuit tuning and input power adjusted to maintain output power of 15 W @ 12.5 Vdc.

*Z$_{OL}$ = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

NORMALIZED TO 10 Ω

V_{CE} = 12.5 VDC, P$_{out}$ = 15 Watts

Figure 26. MRF873 Data Book Input and Output Impedances

CONCLUSIONS

For an RF power transistor we have demonstrated that the input and output large–signal device impedances are not only frequency dependent, but are also determined by the operating conditions of the device. Because of the wide range of possible applications, it is virtually impossible for the device manufacturers to present impedance data for every eventuality. The user, therefore, is left with the choice of either measuring the device impedances under the conditions he plans to use the device, or resorting to the classical methods of tweaking the circuit impedances into approximately the optimum match. The future does hold some promise in two areas. Automated tuners will enable impedance data to be gathered faster, enabling more comprehensive data to be included on the data sheets with the eventual possibility of publishing device impedance distributions. Compact device models in conjunction with non–linear simulators hold the best hope for simulating the device under the proposed operating conditions, and then permitting the software to synthesize the optimum broadband matching networks.

™SuperCompact is a trademark of Compact Software and Touchstone is a registered trademark of EESof, Inc.

APPENDIX I:
Load–Pull Method and Corrections for Power Measurement in Non–50 Ohm Environment

Load–pull measurements can employ a variety of test equipment and methods. For the load–pull measurements described earlier in this paper we used readily available and inexpensive equipment. In addition to the usual equipment found on an RF power bench including a computer as the instrument controller, the only additional pieces of equipment needed are a vector voltmeter, a variety of low attenuation power attenuators, and a variable length shorted stub. Figure 24 shows a block diagram of the bench set–up. A series of load mismatch conditions was established by terminating a broadband test fixture with the attenuators and shorted stub. The shorted stub was calibrated at approximately 20° intervals to establish varying phase shifts. By varying the value of attenuation, a grid of load impedances can be presented to the device on a network of VSWR circles in the reflection coefficient plane. The system was first calibrated by using a network analyzer and a probe in the device socket to measure this series of load impedances. A vector voltmeter, with error correction, could of course have been used to measure these impedances.

After system calibration, the transistor was operated with the drive level adjusted to obtain rated output power under optimum tuning for maximum gain into a matched load. With the drive level fixed at this level, the output power was remeasured over the range of calibrated load impedances. This procedure was repeated at each frequency desired. The input match was tuned for zero reflected power with the output terminated in a matched load. The input return loss, under mismatched conditions, thereby indicates changes in magnitude of the input impedance. In addition to the usual power meter to measure the output power from the test fixture, a vector voltmeter monitors the test fixture load reflection coefficient Γ_L. Standard three term error correction was applied to the measured reflection co–efficient and this value is then used to correct the output power, P_{out}. The system is calibrated over a range of frequencies and the error correction in software.

The following formula can be used to correct the power reading, [16]

$$\Gamma_L = e_{23} + \frac{e_{22}e_{24}\Gamma_M}{1 - e_{21}\Gamma_M} \tag{2}$$

$$P_{out} = P_{om} \bullet |1 - e_{21}\,\Gamma_M|^2 \bullet (1 - |\Gamma_L|^2) \tag{3}$$

where Γ_M is the uncorrected load reflection coefficient,

e_{23}, e_{21}, and $e_{22}e_{24}$ are the directivity, source match and frequency response errors determined by normal vector analyzer correction techniques [32],

and

P_{om} is the measured power meter reading corrected for directional coupler coupling magnitude, attenuation and meter frequency response.

Using this method, accurate measurement of power and hence efficiency can be obtained for a system in which the load impedance is perturbed from the characteristic impedance of the transmission line power meter components. Contours can be generated from this grid data by a number of commercially available software packages.

An alternative system would be to use tuners in place of the attenuator/shorted stub combination. The tuners can be either manual or automated. The advantage of the latter is that with suitable software the de–embedded load impedance presented to the device is available instantaneously. Also, with suitable software, the gain and efficiency circles can be determined by contour following techniques in real time, instead of fitting contours to measurements on a grid of load mismatch points [20].

REFERENCES

(1) K. Kurokawa, "Power Waves And Scattering Matrix," IEEE Transactions on Microwave Theory and Techniques, 194–202, March 1965.

(2) R. J. Frost, "Large–Signal S–Parameters Help Analyze Stability," Electronic Design, 93–98, May 24, 1980.

(3) R. Hejhall, "Small–Signal Parameters Aid FET Power–Amp Design," Microwaves & RF, 141–144, September, 1985.

(4) R. J. Chaffin, and W. H. Leighton, "Large–Signal S–Parameter Characterization of UHF Power Transistors," Digest of Technical Papers, Proceedings 1973 IEEE MTT International Microwave Symposium, University of Colorado, Boulder, June 5, 1973.

(5) L. S. Houselander, H. Y. Chow, and R. Spence, "Transistor Characterization by Effective Large–Signal 2–Port Parameters," IEEE Journal of Solid–State Circuits, SC–5, 77–79, April 1970.

(6) O. Müller, "Large–Signal S–Parameter Measurements of Class C Operated Transistors," Nachrichtentech Z., October 1968.

(7) W. H. Leighton, R. J. Chaffin, and J. G. Webb, "RF Amplifier Design with Large–Signal S–Parameters," IEEE Transactions on Microwave Theory and Techniques, MTT–21, 809–814, December 1973.

(8) S. R. Mazumder, "Two–Signal Method of Measuring the Large–Signal S–Parameters of Transistors," IEEE Transactions on Microwave Theory and Techniques, vol. MTT–26, 417–420, June 1978.

(9) S. R. Mazumder, "Characterization and Design of Microwave Class C Transistor Power Amplifier," Ph.D. dissertation, Carleton University, Ottawa, Canada, 1976.

(10) S. R. Mazumder and P. D. van der Puije, "Characterization of Nonlinear 2–Ports for the Design of Class–C Amplifiers," Microwaves, Optics and Acoustics, vol. 1, No. 4, 139–142, July 1977.

(11) S. R. Mazumder and P. D. van der Puije, "An Experimental Method of Characterizing Nonlinear 2–Ports and Its Application to Microwave Class–C Transistor Power Amplifier Design," IEEE Journal of Solid–State Circuits, vol. SC–12, no. 5, October 1977.

(12) William P. Overstreet and William A. Davis, "Measuring Parameters of Large–Signal Nonlinear Devices," Microwaves & RF, 91–96, November 1987.

(13) R. Hejhall, "Systemizing RF Power Amplifier Design," Motorola Application Note AN–282, Motorola Semiconductor Products, Inc., Phoenix, Arizona, August 1968.

(14) C. W. Bostain, H. L. Krauss, and F. H. Raab, *Solid State Radio Engineering*, John Wiley & Sons, Inc., New York, 1980, pp 406–408.

(15) C. Bowick, *RF Circuit Design*, Howard W. Sams & Company, Indianapolis, 1982.

(16) Rodney S. Tucker and Peter D. Bradley, "Computer–Aided Error Correction of Large–Signal Load–Pull Measurements," IEEE Transactions on Microwave Theory and Techniques, vol. MTT–32, No. 3, March 1984.

(17) Dennis Poulin, "Load–Pull Measurements Help You Meet Your Match," Microwaves, pp. 61–65, Nov. 1980.

(18) Hiroyuki Abe and Yoichi Aono "11–GHz GaAs Power MESFET Load–Pull Measurements Utilizing a New Method of Determining Tuner Y Parameters," IEEE Trans. Microwave Theory and Techniques, vol. 27, no. 5, pp. 394–399, May 1979.

(19) G. P. Bava, U. Pisani, and V. Pozzolo, "Active Load Technique for Load–Pull Characterisation at Microwave Frequencies," Electronics Lett., vol. 18, no. 4, pp. 178–179, February 1982.

(20) Joseph M. Cusack, Stewart M. Perlow, and Barry S. Perlman, "Automatic Load Contour Mapping for Microwave Power Transistors." IEEE Trans. Microwave Theory and Techniques, vol. MTT–22, vol. 12, pp. 1146–1152, December 1974.

(21) David Zemack, "A New Load Pull Measurement Technique Eases GaAs Characterization," Microwave Journal, pp. 63–67, November 1980.

(22) Rodney S. Tucker, "RF Characterization of Microwave Power FET's," IEEE Trans. Microwave Theory and Techniques, vol. MTT–29, vol. 8, pp. 776–781, August 1981.

(23) Yoichiro Takayama, "A New Load–Pull Characterization Method for Microwave Transistors," Proc. IEEE MTT–S, pp. 218–220, June 1976.

(24) A. M. Khilla, "Accurate Measurement of High–Power GaAs FET Terminating Impedances Improves Device Characterization," Microwave Journal, pp. 255–263, 1985.

(25) Roger B. Stancliff and Dennis D. Poulin, "Harmonic Load–Pull," Proc. IEEE MTT–S, pp. 185–187, May 1979.

(26) Ronald R. Bauer and Paul Penfield, "De–Embedding and Unterminating," IEEE Trans. Microwave Theory and Techniques, vol. MTT–22, vol. 3, pp. 282–288, March 1974.

(27) Lawrence Dunleavy and P. B. Katehi, "Eliminate Surprises when De–Embedding Microstrip Launches," Microwave & RF, pp. 117–112, August 1987.

(28) Lance A. Glasser, "An Analysis of Microwave De–Embedding Errors," IEEE Trans. Microwave Theory and Techniques, vol. MTT–26, vol. 5, pp. 379–380, May 1978.

(29) Michael Hillbun, "Compensate Analyzer Errors and De–Embed S–Parameters," Microwaves, pp. 87–92, January 1980.

(30) Richard Lane, "De–Embedding Device Scattering Parameters," Microwave Journal, pp. 149–156, August 1984.

(31) Dan Swanson, "Ferret Out Fixture Errors With Careful Calibration," Microwaves, pp. 79–86, January 1980.

(32) Jim Fitzpatrick, "Error Models for System Measurement," Microwave Journal, pp. 63–66, May 1978.

(33) I. Kasa, "Closed–Form Mathematical Solutions to Some Network Analyzer Calibration Equations," IEEE Trans. Instrumentation and Measurement, vol. IM–23, vol. 4, pp. 399–402, December 1974.

(34) W. Kruppa and K. F. Sodomsky, "An Explicit Solution for the Scattering Parameters of a Linear Two–Port Measured with an Imperfect Test Set," IEEE Trans. Microwave Theory and Techniques, vol. MTT–19, vol. 1, pp. 122–123, January 1971.

(35) Daniel N. Meeks, "Re–Normalizing the Scattering Parameters," RF Design, pp. 41–42.

(36) Stig Rehnmark, "On the Calibration Process of Automatic Network Analyzer Systems," IEEE Trans. Microwave Theory and Techniques, vol. MTT–24, vol. 4, pp. 457–458, April 1974.

(37) H. V. Schurmer, "Calibration Procedure for Computer–Corrected S–Parameter Characterisation of Devices Mounted in Microstrip," Electronics Lett., vol. 9, no. 14, July 1973.

Ⓜ **_MOTOROLA_**   ◊