SHORT AND LONG-TERM SAFE OPERATING AREA CONSIDERATIONS IN LDMOS TRANSISTORS

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[*Keywords:* LDMOS, SOA, hot carrier lifetime, thermal instability, WLR, ESD, CHC lifetime, thermal SOA, electrical SOA]

INTRODUCTION

Lateral DMOS transistors are widely used in mixed-signal IC circuit designs, particularly where power handling is important. Both high-voltage (20 to 100 V) and high current (2 to 3A) output drivers are required for applications within the automotive, paper media, digital audio, and other markets. This paper views the LDMOS from a power-handling perspective, considering both design and characterization aspects.

Safe operating area regimes

In designing and using the LDMOS, particular attention must be paid to the electrical stress placed on this component. If the stress exceeds certain limits, the device is likely to fail. The phrase "safe operating area" or SOA is used to define the boundaries that limit the device operating point to conditions that prevent device failure. Because devices can be stressed in a variety of ways, SOA definition is not straightforward. To help with SOA determination, it makes sense to define not one, but several safe operating areas, distinguishing them mainly by the duration time of the electrical stress. Three different SOAs are indicated in the plot of Figure 1, which shows stress time as the horizontal axis. Electrical and thermal SOAs typically deal with stress times less than a few ms, that is, their boundaries are determined by "short-term" testing. Alternatively, hot carrier stress tests typically require times from a few hundred to several thousand seconds and are labeled "long-term." An important point is that the maximum allowed power density, shown as the vertical axis in Figure 1, depends on stress time and has the general shape indicated in Figure 1.

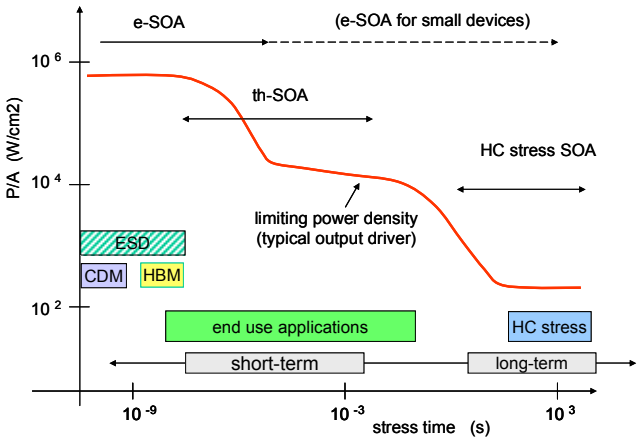

FIGURE 1. MAXIMUM POWER DENSITY *VS.* STRESS TIME FOR A TYPICAL LDMOS, SHOWING VARIOUS SOA REGIMES.

Short-term vs. long-term SOA

Short-term SOA regimes can be linked to two different carrier generation processes that trigger catastrophic device failure [1]. Both impact ionization and thermal generation can create "excess" carriers within the device. The carriers are labeled excess because they provide currents that are not under gate control. If these excess currents reach levels comparable to the current being controlled by the gate, instability and device failure can occur.

Rather than detecting catastrophic device failure, hot carrier stress tests monitor degradation of some fundamental device parameter, for example, on-resistance, *Rdson,* or threshold voltage. The degradation is associated with trapping of impact generated carriers at the oxide/Si interface under the gate or within the drift region [2], [3], [4]. Impact ionization dominates electrical and HC stress safe operating areas and can play a secondary role in thermal SOA. Thermal generation is mainly associated with thermal SOA.

HIGH-VOLTAGE MOS TRANSISTORS

Conventional MOS transistors are generally not useful for processing power. They are designed instead to process information (bits) using minimum input energy while occupying the least area. Gate lengths are minimized as is gate oxide thickness. Figure 2 shows a simplified cross-section of a conventional NMOS transistor.

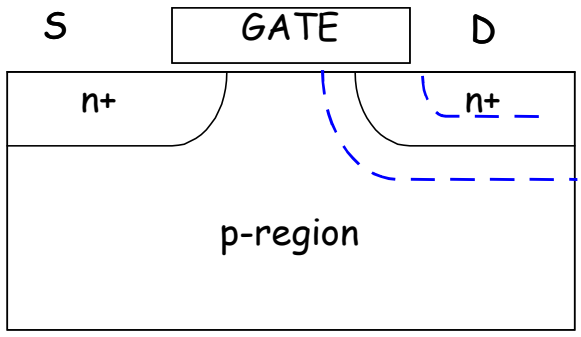

FIGURE 2. NMOS CROSS-SECTION WITH APPLIED V_{DS} AND WITH V_{GS}=0. THE DRAIN DEPLETION LAYER IS INDICATED BY THE DASHED LINES.

Maximum drain voltage is limited by gate oxide breakdown as well as by the combined effects of punch-through and avalanche breakdown from drain-to-source. CMOS technologies currently have maximum drain voltages moving into the 1 to 2 V range. This means that changes need to be made to conventional NMOS and PMOS geometries if they are to handle power.

Extending the drain

By interposing a lightly-doped n-type gap between drain and gate, the drain voltage can be increased. The idea is to avoid exceeding the silicon critical electric field, *Ecrit,* while increasing drain-gate distance just enough to reach the required voltage. *Ecrit* ranges from 10 to 30 V/μm and depends on how well parasitic npn action is suppressed [1]. Figure 3 illustrates a "drain extended" NMOS or DENMOS. In many cases, the positive charge in the depleted n-region can be balanced by the negative charge in the p- layer underneath. With this approach, "RESURF" (reduced surface field) [5], [6] action becomes possible. The electric field becomes nearly horizontal and fairly uniform along the low-doped region. By maintaining charge balance and using the appropriate vertical profiles, the maximum *Vds* can be increased simply by increasing the length of the low-doped region. One negative consequence of this approach is increased *Rdson*. The drain Nwell can usually be used to provide the drain extension, but in some cases an extra mask may be needed.

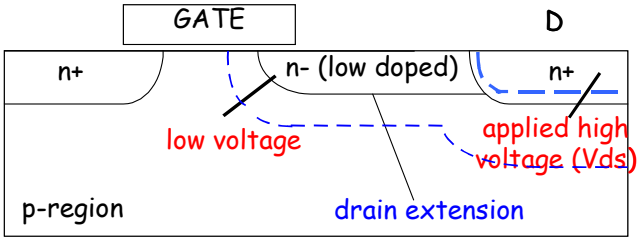

FIGURE 3. DRAIN-EXTENDED NMOS (DENMOS) CROSS-SECTION. THE ENTIRE LOW-DOPED REGION IS DEPLETED.

The Lateral DMOS

One difficulty with the DENMOS is that the gate length needs to be fairly long to avoid punchthrough. This is due to the relatively light doping of the p-region under the gate. By adding a mask and implant step that increases this doping to form a laterally diffused "body" region beneath the gate, one can create a lateral DMOS or LDMOS. The LDMOS can have channel lengths an order of magnitude less than a DENMOS. This means that it is possible to significantly reduce device area, while achieving low channel resistance and a corresponding favorable increase in trans-conductance. The penalty is a moderate increase in threshold voltage, which is usually acceptable in power applications.

Figure 4 shows the cross-section of one style of lateral DMOS. In this case the gate and drift region are both confined to the thin oxide or active region, forming an "active-gap" LDMOS.

A second style of LDMOS, which has a "field-gap," is shown in Figure 5. In this case, the gate is extended over the thick field-oxide, thereby providing a field-plate that reduces junction curvature effects. The field-gap style is preferred for voltage ratings above 20 to 30V.

Figure 6 summarizes the main features of the DEMOS and LDMOS. In general, for high-voltage, low-current applications, the DEMOS, is preferred. Where both high-voltage and high-current are required, the LDMOS is the preferred device. For this reason, it is usually the LDMOS that leads to questions about safe operating area, which is discussed in the next section.

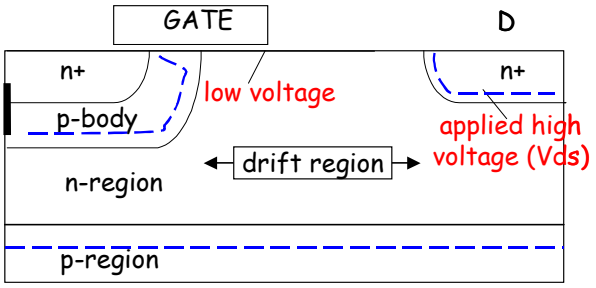

FIGURE 4. CROSS-SECTION OF AN ACTIVE-GAP LATERAL DMOS. THE P-BODY IS SELF-ALIGNED TO THE SOURCE OR GATE EDGE.

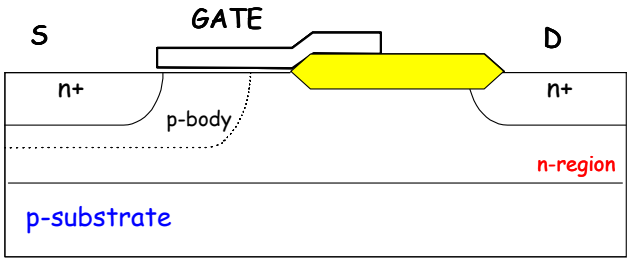

FIGURE 5. CROSS-SECTION OF A FIELD-GAP LDMOS. THE GATE OVERLAPS THICK FIELD OXIDE.

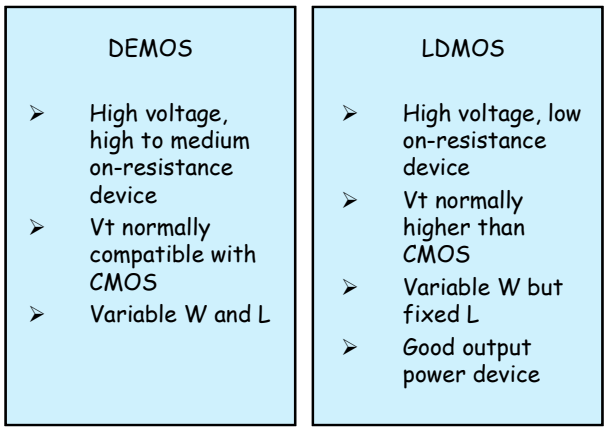

FIGURE 6. COMPARISON OF DRAIN EXTENDED MOS TRANSISTORS AND LATERAL DIFFUSED MOS TRANSISTORS. THE OBSERVATIONS APPLY TO BOTH P AND N-CHANNEL.

SHORT-TERM LDMOS SAFE OPERATING AREA

Undesired turn-on of the parasitic bipolar that exists in parallel with the LDMOS can lead to the device suddenly switching to a low-impedance state. Although the triggering of device failure is an *electro-thermal* event, it is usually the case that one mechanism dominates. Therefore it is convenient to think of the overall SOA as being the combination of a thermal SOA and an electrical SOA [1].

SOA boundary conditions

The electrical SOA boundary is where the device begins to exhibit negative resistance. The resulting "snapback" to a low-voltage state is rapid and occurs within tens of pico-seconds. In some

cases, the LDMOS is able to survive the transition to the low-impedance state [7], however, the snapback event is disruptive to circuit operation. Therefore the safe operating boundary is defined to be at the onset of negative resistance. Within the device, electrical SOA can be characterized by the field at the drain contact reaching a critical value, *Ecrit*. From the standpoint of terminal conditions, electrical SOA is best represented by a curve in the *Id, Vds* plane. Electrical SOA is discussed further in a later sub-section.

The thermal SOA boundary is defined by the device being on the verge of thermal instability or thermal runaway, where the thermal instability is brought about by LDMOS self-heating. In some cases, LDMOS self-heating can be assisted by impact generated drain current [8], however, the triggering mechanism is still dominated by thermal instability. The thermal SOA boundary can be characterized by the junction reaching a critical temperature, *Tcrit*. As described in the next sub-section, this temperature can be extracted from measured power-pulse failure points using a model of device thermal resistance that corresponds to the measurement pulse time. With *Tcrit* and thermal resistance *Rth(tp)* known, any power pulse can be checked to see whether it exceeds the thermal SOA.

Determining thermal SOA

Figure 7 shows electro-thermal simulation results for temperature and drain current per unit gate width, for a 60V LDMOS. A power pulse of *Vds*=50V and *Vgs*=4V is applied. Initially, the junction temperature shows the usual parabolic response associated with thermal diffusion. After about 80µs, the device exhibits thermal runaway of drain current at a junction temperature near 800K. Please note that at the beginning of the pulse, the drain current temperature coefficient is negative, corresponding to a thermally stable situation. Nevertheless, as time (and temperature) increases, a point is reached where the temperature coefficient changes sign and becomes positive, leading eventually to thermal instability.

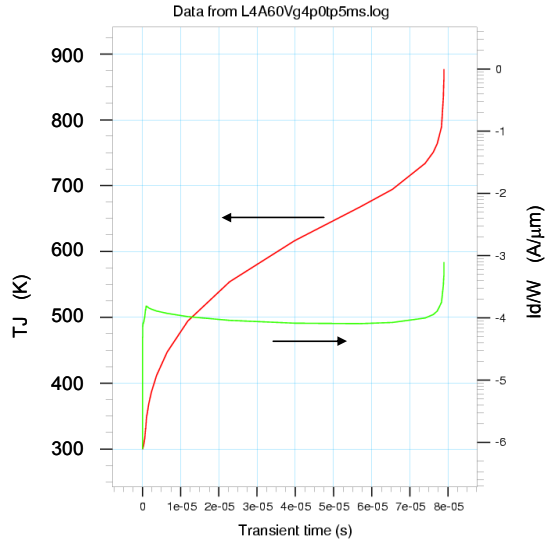

FIGURE 7. SIMULATED JUNCTION TEMPERATURE AND NORMALIZED DRAIN CURRENT VS. TIME IN RESPONSE TO AN APPLIED POWER PULSE.

Figure 8 shows a plot of "measured" *Tcrit* vs. drain-source voltage for LDMOS from two different power IC technologies. For these measurements, low duty cycle *Vds* pulses (1ms) are applied, and *Vgs* is gradually increased until thermal runaway is detected at the end of the pulse. For example, see [9] for a test circuit and waveform examples. For a given pulse, *Tcrit* is calculated using a thermal model of the device, [8],[10]. As shown in the plots of Figure 8, there is some variation of *Tcrit* with *Vds* and also between the two types. For large *Vds*, impact ionization provides carriers (holes) that act as base drive for the parasitic npn, enhancing npn turn-on, and thereby reducing *Tcrit*. This effect is less pronounced in the Type B LDMOS due to improved shorting of the base-emitter junction of the parasitic npn. At lower *Vds,* there is a notable increase in *Tcrit* for both LDMOS. Based on preliminary simulation studies, this increase appears to be due to the ballasting effect of npn emitter/source resistance. Further work is needed to fully understand the shape of the *Tcrit* curve at low *Vds*.

Independent of these interesting physical explanations, the *Tcrit vs. Vds* curve and the LDMOS thermal model provide useful tools for predicting thermal SOA without the need of building prototype devices. The advantage of using *Tcrit* for device design is that it is essentially independent of device size and pulse time.

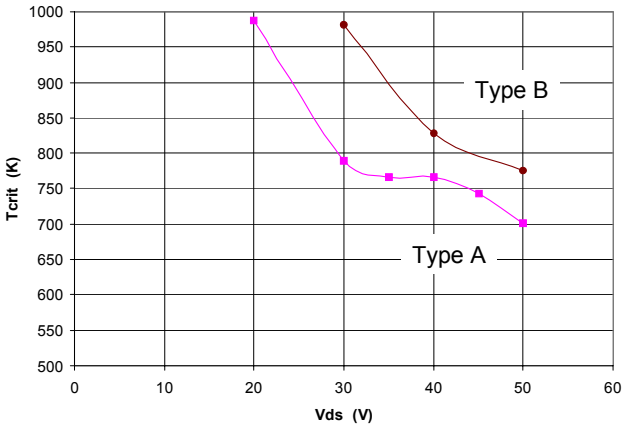

FIGURE 8. CRITICAL TEMPERATURE VS. DRAIN SOURCE VOLTAGE FOR 50V LDMOS FOR TWO DIFFERENT DESIGNS. *TCRIT* IS EXTRACTED FROM 1 ms PULSE MEASUREMENTS.

Electrical SOA

Figure 9 depicts electron flow within the drift region. The situation can be approximated by assuming that there is a pseudo one-dimensional "flux tube" within the drift region. Electrical instability can arise when both Vds and current density within the drift region are sufficiently high [11].

When the current density exceeds a value given by the average doping in the drift region, negative charge from the electrons shifts the slope of the field profile within the flux tube. This action is illustrated at the top of Figure 9, where the dashed line shows the field profile at low currents. The solid line shows the profile for the case where the current is large enough to tilt the profile and where *Ecrit* is reached at the drain contact. In the latter state, increasing current density leads to decreasing voltage and the device is in a negative resistance or snapback mode. Electrical SOA limits apply, provided temperatures do not rise to the point of initiating thermal instability. Electrical SOA is appropriate for an ESD HBM event (~100ns pulses) or during reverse recovery of a body diode in an H-bridge, where recovery times are typically in tens of nano-seconds.

Examples of measured electrical SOA are shown in Figure 10. For these measurements a transmission line pulse technique (TLP) is used, where pulses are applied drain-to-source and *Vgs* is held constant [1]. The pulse time is 100ns. Each point on the curve corresponds to the onset of snapback for a particular value of *Vgs*. It can be seen that there is a major improvement in e-SOA for the Type B LDMOS. This increase is directly related to the lower base-emitter resistance shunting the npn, which permits an effective increase in *Ecrit* [12]. The on-resistance, area product (*Rsp*) of these two LDMOS is about the same.

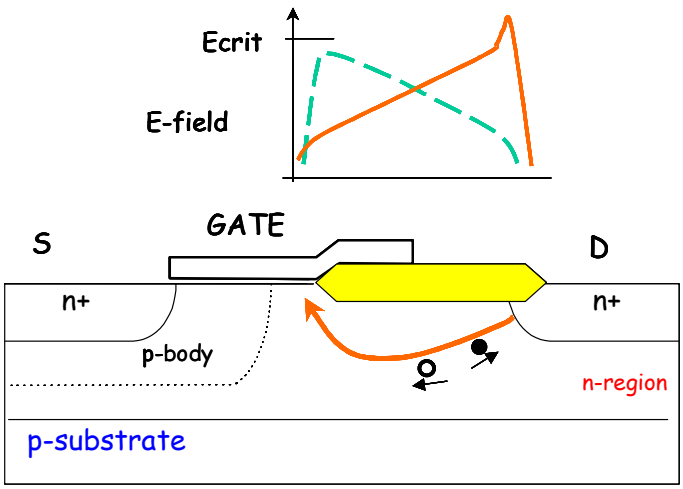

FIGURE 9. LDMOS CROSS-SECTION SHOWING THE FLOW PATH FOR CONVENTIONAL CURRENT AND FOR ELECTRONS AND HOLES WITHIN THE DRIFT REGION. THE DASHED FIELD PROFILE IS AT LOW CURRENT DENSITY AND THE SOLID IS AT HIGH CURRENT DENSITY.

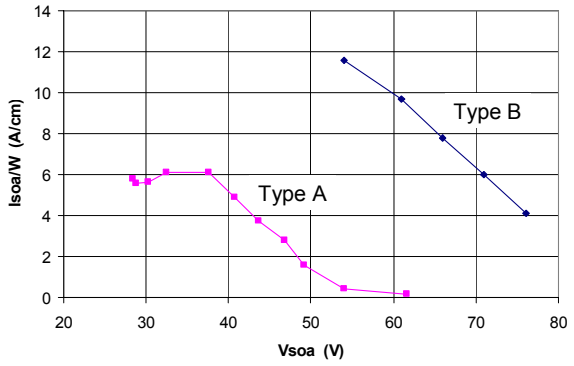

FIGURE 10. MEASURED SNAPBACK DRAIN CURRENT VS. DRAIN VOLTAGE AS OBTAINED FOR DIFFERENT *VGS*. THE CURVES DEFINE THE ELECTRICAL SOA FOR TWO DIFFERENT 50V LDMOS. DRAIN CURRENT IS NORMALIZED TO GATE WIDTH.

In the plots of Figure 10, drain current is normalized to gate width, *W*. From experimental measurements on devices having a wide range of gate widths, we know that these curves are essentially independent of *W*. Thus data similar to that of Figure 10 can be used to scale devices to meet a particular electrical SOA requirement. Again, the need for building prototype devices is substantially reduced by using this type of curve.

LONG-TERM LDMOS SAFE OPERATING AREA

Since current flow and impact generation in LDMOS devices can be close to the semiconductor-dielectric interface, high electric fields can impart sufficient energy to the carriers so that they overcome the energy barrier at the interface and get injected into the dielectric. This hot carrier injection can significantly affect the device performance. Although it is not a catastrophic failure, device operation is limited to prevent any significant degradation due to hot carrier injection (HCI). The operating regime so defined is called *hot carrier stress SOA (HCSOA)*.

Hot carrier stress SOA

HCSOA for an LDMOS device is generally limited by degradation in on-state resistance for high drain and low to medium gate voltage conditions and by degradation in threshold voltage for high gate voltage bias conditions.

Degradation in the threshold voltage (*Vt*) depends upon the resistance of the source link, which is the lightly doped region connecting the channel to the heavier doped source region. As shown in [4], *Vt* degradation can be substantially improved by using a lower resistance source link. Such a low resistance source link may not be always compatible with the lightly doped regions used in NMOS devices and may need additional processing.

Rdson degradation

Degradation mechanisms affecting the on-state resistance of the LDMOS are addressed in greater detail in this sub-section. Figure 11 plots the impact ionization contours and potential distribution for an active-gap LDMOS device for "worst" case stress condition. The worst case stress condition is defined as the bias condition causing the most degradation in *Rdson*. As seen from Figure 11, the high electric field near the surface causes significant impact generation close to the interface.

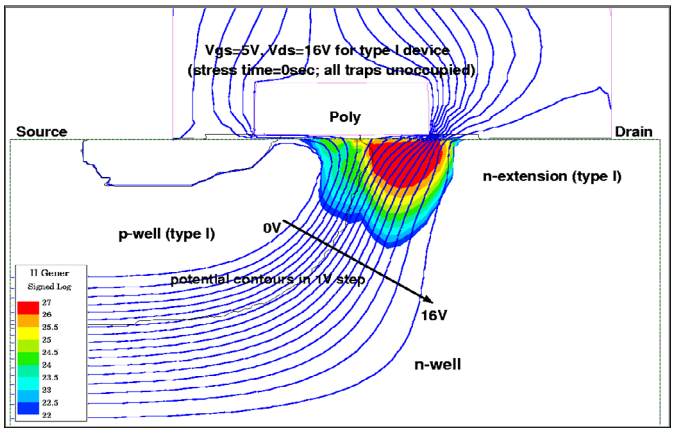

FIGURE 11. IMPACT IONIZATION CONTOURS AND POTENTIAL DISTRIBUTION FOR WORST CASE STRESS CONDITION.

Two dimensional simulations of the device structure, including traps in the dielectric, show that the observed degradation in *Rdson* is

due to the electron capture by traps in the dielectric area over the drift region but close to the gate oxide area [2]. This is shown in Figure 12 below. It is proposed in [3] that these traps are generated due to hot hole injection when the device is operating at high voltage and high current conditions.

Since the *Rdson* degradation primarily occurs due to hot carrier injection near the gate-edge – drift-region boundary, the HCSOA of the LDMOS is critically dependent on the drain engineering of the device. The doping profile in the drift region and particularly in the region under the thin gate oxide has a significant influence on the HCSOA. Optimizing this profile can substantially reduce the hot carrier injection and associated degradation and improve the overall HCSOA as shown in Figure 13 below.

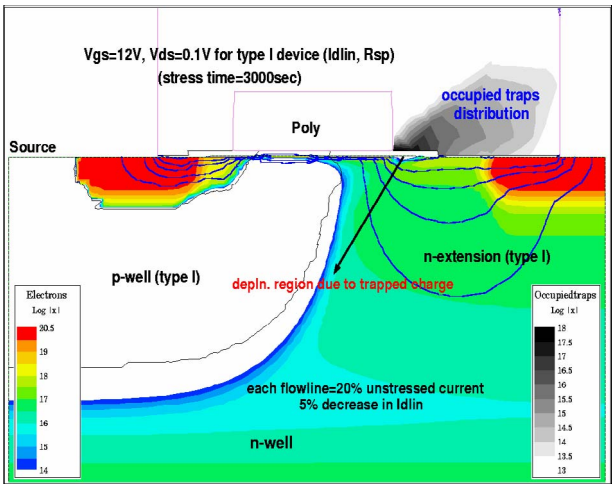

FIGURE 12. ELECTRON DISTRIBUTION, CURRENT FLOWLINES AND TRAPPED CHARGE DISTRIBUTION SHOWING ~5% DEGRADATION IN RDSON AFTER 3000 SECOND STRESS TIME.

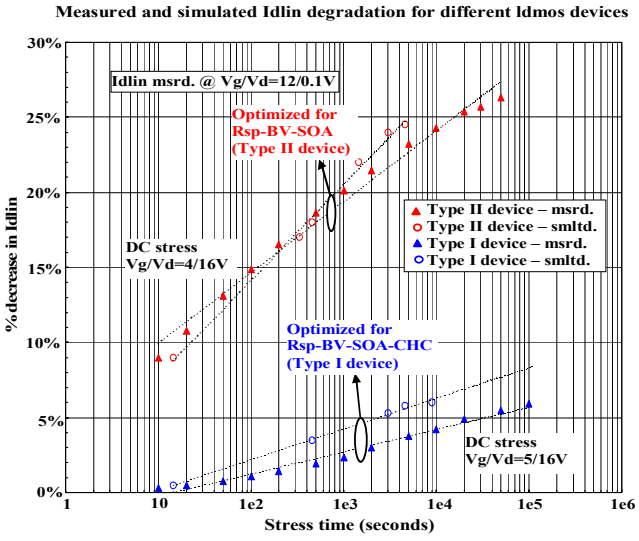

FIGURE 13. MEASURED AND SIMULATED IDLIN DEGRADATION FOR LDMOS DEVICES WITH DIFFERENT DRAIN ENGINEERING. THE TYPE I DEVICE SHOWS SATURATION IN DEGRADATION (<10% DEGRADATION FOR 10 YEAR OPERATION. (IDLIN IS MEASURED AT V_{DS}=0.1V AND IS EQUIVALENT TO MEASURING R_{DSON}).

The plots of Figure 13 show that the Type I device gives much less degradation than the Type II device and therefore has a superior HCSOA. The main difference between the two types is that for Type II, the drain extension is a shallow implant inside Nwell, while Type I uses a deeper drain extension [2]. The deeper drain extension in the Type I device diffuses significantly more under the thin gate oxide region. This not only reduces the number of injected carriers in the drift region but also allows the channel electrons in Type I device to spread out deeper as they enter the drift region. The deeper current flow results in less influence of the injected carriers causing a much lower degradation in Type I on-state resistance.

It should be noted that although the data for an active-gap 16V rated LDMOS is shown here, the device behavior and degradation mechanisms are generally similar for field-gap LDMOS devices.

OVERALL LDMOS SAFE OPERATING AREA CHARACTERIZATION

In order to minimize the intrinsic base resistance and improve the device robustness, LDMOS devices normally use "integrated" source / p-body contact strategy. For this reason, the body current cannot be directly measured in these devices. This, coupled with the fact that the hot carrier degradation in these devices does not follow the same "degradation *vs.* Isub" power law relationship as in a standard NMOS, means that HCSOA characterization has to be done differently for LDMOS devices. The HCSOA characterization typically includes stressing the device at multiple drain and gate voltages and then extrapolating to find the time for degradation by a predetermined amount (usually 10% of the unstressed value). This data can then be combined along with electrical SOA characterization data to create a SOA plot in the Vds – Vgs plane.

Figure 14 and Figure 15 show combined SOA plots for the two types of LDMOS shown in the previous section. Different color coding or shading is used to identify the regions suitable for analog and digital operation. Digital operating region is then further sub divided depending upon allowed duty cycle. The overall improved SOA of the Type B LDMOS device can be readily seen from these plots.

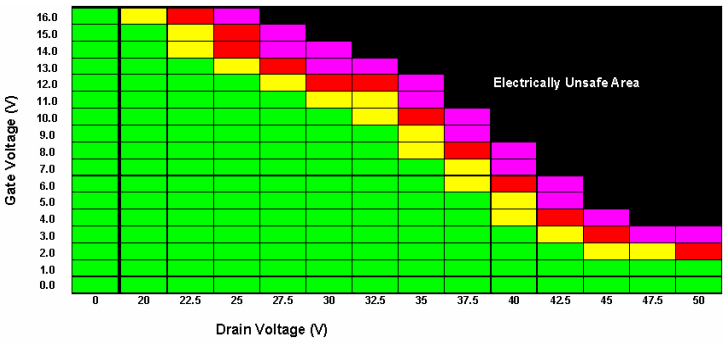

FIGURE 14. TYPICAL SOA PLOT FOR A TYPE A LDMOS DEVICE COMBINING HCSOA AND E-SOA. THE ALLOWED DUTY CYCLE PROGRESSIVELY DECREASES GOING FROM LEFT TO RIGHT. THE DEVICE FAILS CATASTROPHICALLY IF OPERATED IN THE REGION DENOTED AS "ELECTRICALLY UNSAFE"

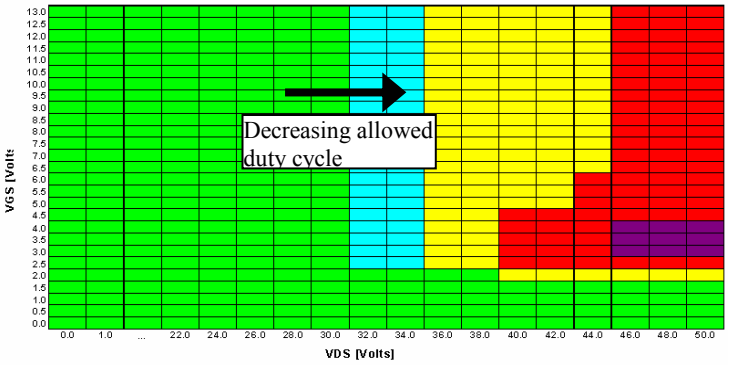

FIGURE 15. TYPICAL SOA PLOT FOR A TYPE B LDMOS DEVICE COMBINING HCSOA AND E-SOA. OVERALL SOA FOR THIS DEVICE IS SIGNIFICANTLY IMPROVED COMPARED TO TYPE A LDMOS DEVICE FROM FIGURE 14.

CONCLUSIONS

The complex nature of LDMOS safe operating area can be dealt with by considering long-term and short-term operating conditions. Long-term conditions are covered by a hot carrier SOA, and short-term conditions are further sub-divided into electrical SOA and thermal SOA. Characterization examples of the various kinds of SOA have been given in the paper. Criteria for meeting a required SOA have also been described. O*ptimization* of an LDMOS design to meet SOA requirements while minimizing device area is a more complicated situation and has not been described here.

Traditionally, the *Rsp* (specific on-resistance) – *BV* relationship has been used as a Figure of Merit (FOM) for LDMOS devices. Numerous advances in device design have been reported looking at improving the *Rsp – BV* tradeoff, however, this only treats one aspect of the overall LDMOS design opportunity. With continuously shrinking geometries and gate dielectric thicknesses, device performance is also being limited by the short-term electro-thermal and long-term HCSOA requirements. Hence LDMOS device design needs to look at the more complicated 4-way optimization between *Rsp, BV*, short-term and long-term SOA.

ACKNOWLEDGMENTS

Thanks are due Robert Higgins and Rene Chan from the WLR laboratory for providing HCSOA data. Michelle Arguin assisted with TLP and other electrical measurements. Helpful comments and suggestions have been provided by John Lin, Steve Merchant, Sheldon Haynie, Rob Shaw, Jeff Smith, and Lou Hutter.

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