Switched Doherty PAs for 3G

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Outline

• Introduction and motivation
• Pros and Cons
• Background: Stepped bias and switched periphery
• Switched Doherty
• Example PAs
• Performance improvement techniques
• Test data
• Tristate switched Doherty PA in BiHEMT process
• Conclusion
Why Use Switched Doherty PAs?

• CDMA talk-time is strongly influenced by PA current
• Average PA current is dependent on power efficiency at low power levels (in addition to full power PAE)
• Improvement in low power PAE requires:
  – a reduction in supply voltage OR
  – an increase in load impedance (compared to full power levels)
• Load impedance can be changed explicitly (switched) or implicitly (periphery switching)
• The results reported here use implicit load control to improve low power efficiency
Pros and Cons

• Switched Doherty PAs are not easy to implement
  – Z inverter (Zo and insertion phase)
  – Delay line (Zo and insertion phase)
  – Interstage branch impedances
  – ALL MUST BE CORRECT - consistent with final stage segmentation

• Performance advantages include:
  – High PAE in both low and high power modes
  – No insertion phase discontinuity during mode change
  – Increased load insensitivity and superior 3rd order reverse IMD due to quadrature operation in high power mode
  – All periphery is used in high power mode
  – External load impedance is same as conventional PA
Background: Conventional PA with Stepped Bias

- 1st GENERATION
  CONVENTIONAL PA
- 1-BIT CONTROL
- ONLY DC QUIESCENT REDUCTION IN LOW MODE
- POOR LOW MODE PAE DUE TO MISMATCH

\[ RF_{input} \rightarrow \text{BASE BIAS-1} \rightarrow + V_{reg} \rightarrow \text{Hi/Lo Step} \rightarrow \text{BASE BIAS-2} \rightarrow + V_{reg} \rightarrow Z_{Load} \rightarrow RF_{output} \]
Background: Conventional PA with Switched Periphery

- 2nd GENERATION CONVENTIONAL PA
- 1-BIT CONTROL
- BETTER LINEARITY IN LOW MODE THAN STEPPED BIAS
- POOR LOW MODE PAE DUE TO MISMATCH

TQ7634
Switched Periphery Load Sharing

HIGH POWER MODE

LOW POWER MODE
Switched Doherty Load Sharing

HIGH POWER MODE

LOW POWER MODE
CDMA Load Sharing Prototype

HIGH POWER MODE

LOW POWER MODE
Constant-K LC Impedance Inverter

\[ L = \frac{Z_0}{\omega_0}, \quad C = \left( \omega_0 Z_0 \right)^{-1} \]
M-derived LC Impedance Inverter

\[ L = \frac{Z_0}{\omega_0}, \quad L_s = \frac{Z_0(3\omega_0)}{-1}, \quad C_s = \frac{3(4\omega_0Z_0)}{-1} \]

TRAP RESONANCE SET TO 2\textsuperscript{nd} HARMONIC
Switched Periphery to Switched Doherty

SWITCHED PERIPHERY

SWITCHED DOHERTY
Switched Doherty PA
Low Power Mode
Low Power Mode

RF output
RF input
+ Vreg
+ Vcc
BASE BIAS-1
BASE BIAS-2A
INVERTER

OPTIMUM PERIPHERY
AND
OPTIMUM LOAD

RF output
+ Vreg
BASE BIAS-1

RF input
Contrast with Other Techniques

SWITCHED DOHERTY IS DUAL PATH SPECIAL CASE

DUAL PATH ARCHITECTURE

BASE BIAS-2A
BASE BIAS-2B
RF output (~ 4 \( \Omega \))

Z_0 \sim 17 \( \Omega \)

HIGH POWER MODE

BASE BIAS-2A
BASE BIAS-2B
OFF OFF
RF output (~ 4 \( \Omega \))

Z_L \sim 70 \( \Omega \)
Contrast with Other Techniques (continued)

DISTORTION IN HIGH POWER MODE

SWITCHED DUAL PATH
Isolation at Interstage Split

**NO ISOLATION**

**WITH ISOLATION**
PCS 1\textsuperscript{st} Generation Switched Doherty

- 1120 x 1200 \text{um}^2
- 6480 \text{um}^2 final
- 550 \text{um}^2 driver
- external 2\textsuperscript{nd} harmonic tuning
PCS 2\textsuperscript{ND} Generation Switched Doherty

- 1170 x 1230 um\textsuperscript{2}
- 6480 um\textsuperscript{2} final
- 550 um\textsuperscript{2} driver
- internal 2\textsuperscript{nd} harmonic tuning
Cellular 2\textsuperscript{ND} Generation Switched Doherty

- 1120 x 1470 \text{um}^2
- 6480 \text{um}^2 final
- 550 \text{um}^2 driver
- internal 2\textsuperscript{nd} harmonic tuning
FISHBONE BASE Geometry for Low $C_{BC}$

- 75% of STANDARD CELL $C_{BC}$
- 57% of HAIRPIN CELL $R_b'$
- SOA is 2X HAIRPIN CELL
- >1 dB gain increase
- >2 % $\eta_a$ increase
Low Inductance Base Manifold

- Lateral manifold contributes to $L_B$
- A low Zo transmission line can reduce $L_B$
- This is realized with $\text{METAL-2/BCB/METAL-1}$ stack
- Increased shunt capacitance is parasitic result
- Lumped equivalent model is convenient
Low Interconnect L from Low Zo Lines

**CHARACTERISTIC Zo**

- 100 um GaAs
- 1.3 um BCB

**INCREMENTAL L and C**

- 100 um GaAs
- 1.3 um BCB
Low Zo Base Manifold - PCS Band

LOW POWER CELLS

HIGH POWER CELLS
Low Zo Base Manifold - Cellular Band

HIGH POWER CELLS

LOW POWER CELLS
Improved Inductors

- Standard overlay increases L but losses Q
- Split and split-overlay increase Q
- Split singles lose area efficiency
- Split-overlay and hybrids are the best overall for good Q with area efficiency

**Split Line Spiral Single Layer**

**Broadside Coupled Split Line Spiral**
Cellular CDMA Performance
PCS CDMA Performance

![Graph of PAE and ACPR vs Output Power (dBm)]

- **PAE (PCS CDMA, High)**
- **PAE (PCS CDMA, Low)**
- **ACPR (PCS CDMA, High)**
- **ACPR (PCS CDMA, Low)**

**Output Power (dBm)**

**ACPR @ 1250 KHz (dBc)**

- 0 dBm
- -10 dBc
- -20 dBc
- -30 dBc
- -40 dBc
- -50 dBc
- -60 dBc
- -70 dBc
UMTS Cellular WCDMA (Rel.99)
UMTS PCS WCDMA (Rel.99)
UMTS Cellular WCDMA (HSDPA)
UMTS PCS WCDMA (HSDPA)
Improvement: Tristate Switched Doherty

- Tristate (2-bit) power control.
- Build on switched Doherty (2-state) core
- No Vref needed -- PA operates directly from Vbatt.
- Enabled with logic interface (< 100uA control)
- Back compatible into standard sockets Vref pin is replaced by “ENABLE” logic input.
- Quiescent currents:
  - 6 mA ! ultra low power mode,
  - 25 mA low power mode, and
  - 78 mA high power mode.
BiHEMT process enables integrated solution:

- Switched Doherty PA core in HBT
- $V_{\text{REF}}$ elimination with pHEMT current sources for HBT bias circuits
- Low current logic pHEMT
- RF switch in pHEMT
BiHEMT: Co-integration of HBT and pHEMT
Tristate PA Module with pHEMT and HBT Chips
HBT PA Size Reduced from Original Switched Doherty

- Builds on original architecture
- HBT PA area is substantially reduced due to removal of complex bias and control circuitry
- Type-1 or type-6 current mirrors are designed to be driven by the Bias-Control chip
Switched Doherty PA Core (2 state)
Tristate Switched Doherty PA
Ultra-Low Power Mode
Simplified View of RF Loading in Tristate PA

- Switched Doherty 2-state core
- Ultra-low power mode uses load from low power mode
- RF input switch drives single cell in ultra-low mode
Separate pHEMT and HBT Chips

pHEMT BIAS / CONTROL

HBT POWER AMPLIFIER
Bias Control ⇒ PA Interface

E/D pHEMT

to RF_in 2

to RF_in 1

ULP mode bias

HBT PA BIAS CIRCUITS

Stage-2A bias

Stage-1 bias

Stage-2B bias
E/D pHEMT Bias Control with HBT PA

ENABLE

E/D pHEMT Bias Control with RF Input Switch

MODE (2)

MODE (1)

InGaP HBT PA Bias Mirrors

Vbe 1 REF

Vbe 2A REF

Vbe 2B REF

Vbe ULP REF

I1 REF

I2A REF

I2B REF

IULP REF

+ VBATT

RF IN

OUT-2

OUT-1

Vbias (to HBT)
Standard HBT Bias Reference Circuits

V_{REF} required in each case
Elimination of $V_{REF}$

- Current density is mirrored in RF (biased) device
- $I_{REF}$ set by $(V_{REF} - V_{be})/R_{SENSE}$
- Precise control of $V_{REF}$ required
- Low $Z_{SOURCE}$ requires high $I_{MIRROR}$ (and high $I_{REF}$)

TYPE-I BIAS MIRROR REFERENCE CIRCUITS

- Current density is mirrored in RF (biased) device
- $I_{REF}$ set by independent of $V_{REF}$ by current source
- Low $Z_{SOURCE}$ is easily obtained since current flows from $V_{cc}$ ($V_{BAT}$)
Current Sources for Bias Circuits

- pHEMT $I_{\text{MAX}}$ is well behaved (epi dependent)
- $\sigma < 7\%$  ($3\sigma = 20\%$)
- Geometry scaled to set current
I₉ Pull-up for Imax Operation of Reference FET

- I₉ < 1 μA
- I₉ is dependent on Iₐss (a wide distribution)
- σ = 16%  (3σ = 48%)
- Tight control of I₉ is not important
PA Enable

- $V_{REF}$ PIN used
- Logic interface
- $V_{REF}$ not needed

![Graph showing current vs enable voltage for different operating temperatures](image-url)

Legend:
- -10C ULP
- +30C ULP
- +90C ULP
- -10C LP
- +30C LP
- +90C LP
- -10C HP
- +30C HP
- +90C HP
Ultra-Low Mode Quiescent Current

SN (All) Vmode1 (V) 3.00 Vmode2 (V) 3.00

I_total (mA)

Vbatt-2 (V)

Vcc1, Vbias, Venable (V) Temp (C)
Tristate Switched Doherty PA Data

- Switched Doherty performance extended to ultra-low power mode
- Quiescent current typically below 6 mA in ultra-low mode
- Ultra-low mode supports up to +12 dBm with -40 dBc ACPR
BiHEMT Tristate Switched Doherty

1st GENERATION SWITCHED DOHERTY CORE

2nd GENERATION SWITCHED DOHERTY CORE
Conclusion

- Switched Doherty PAs have been realized in both PCS and Cellular bands for linear operation.
- Power efficiency and linearity are quite good in both high and low power operation.
- Basic switched Doherty architecture has been extended to Tristate operation with extremely low quiescent current in the lowest power mode.
- BiHEMT process enables integration of pHEMT and HBT circuitry in Tristate PA.
- Several techniques to improve performance have also been presented:
  - A new HBT geometry provides reduced $C_{BC}$
  - Use of low Zo interconnect structures to reduce inductance in base feed manifold
  - Use of composite split-line and overlay (broadside coupled) inductors for better area efficiency and good Q.
- CDMA talk-time is significantly increased.
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