

A COMPACT, HIGH GAIN, 2-20GHz MMIC AMPLIFIER*

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ABSTRACT

Rapid maturing of MMIC technology during the past few years, both in process and design tools, has allowed greatly increased circuit densities while achieving high performance levels. This trend has been key to realizing full cost/performance benefits inherent in MMIC technology.

This paper describes an advanced MMIC amplifier providing a 20 dB gain block over the 2-20 GHz frequency range. The chip requires only three external bias capacitors and is well suited to automatic assembly. By simultaneously offering improved gain, power, and circuit density in the 2-20 GHz range, a significant advancement in single chip performance has been achieved.

INTRODUCTION

Broadband gain chips have been a subject of interest for some time [1,2,3, and 4]. Previous efforts have been compromises between gain power and noise figure. Most efforts have lacked adequate attention to integration of bias circuitry. To provide systems acceptance, the challenge is to simultaneously provide superior gain, power, and noise performance within an affordable chip area. Affordability also requires integrated bias circuitry for low cost assemblies. Goals in the TMM9001/TMM9002 development were targeted to meeting these requirements.

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The TMM9001/TMM9002 chips are shown in Figures 1 and 2. Two foundry design were executed. The TMM9001 was designed for the TI process and the TMM9002 in the Raytheon process.

Topologically, the chips have three stages of distributed amplification. The first two stages use dual gate FETs (four cells/stage), while the TMM9001 final stage is comprised of three cells with single gate FETs (TMM9002 utilizes dual gate FETs in the final stage).

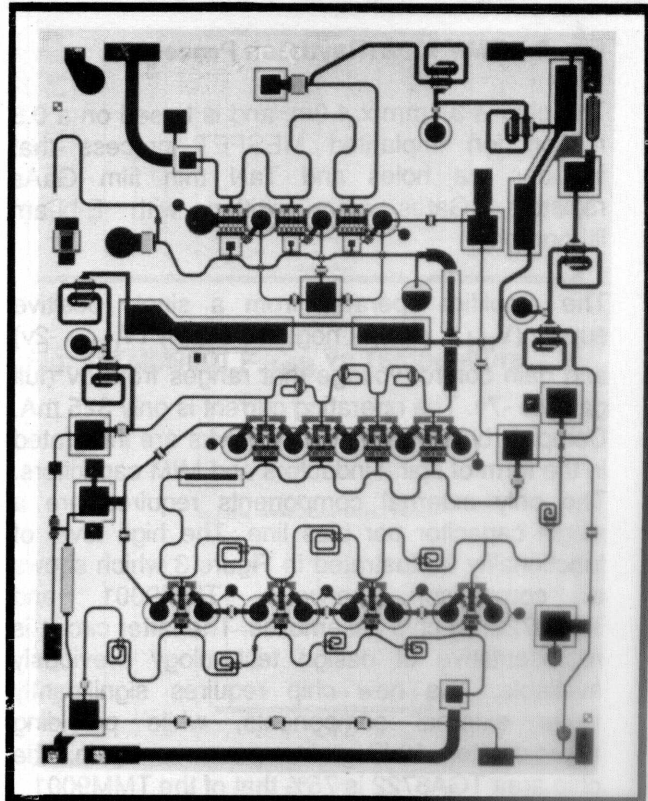


Fig. 1 TMM9001 Wideband Driver (TI Process).

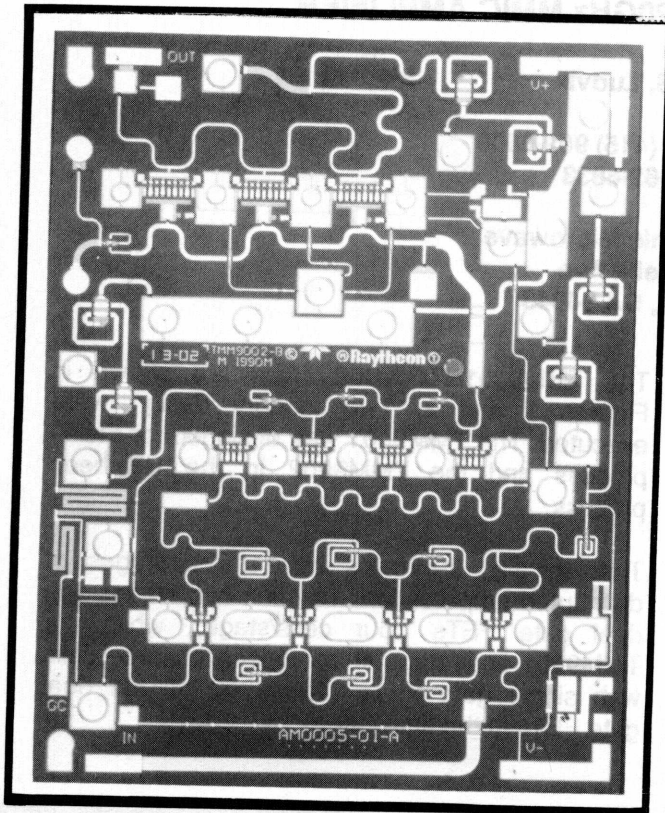


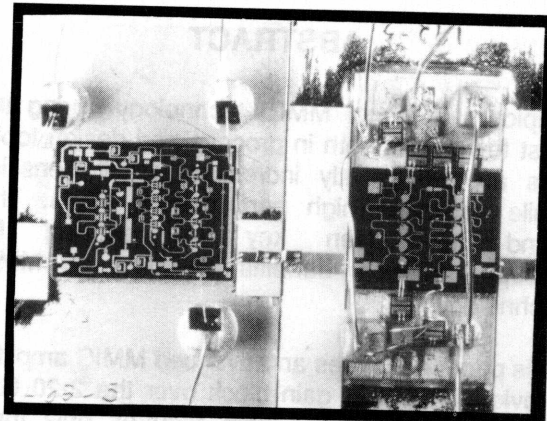
Fig. 2 TMM9002 (Raytheon Process).

The chip is 3.1mm x 4.0mm, and is based on a 0.5 micron ion implanted MESFET process that includes via holes and TaN thin film GaAs resistors. Gates were written with E-beam lithography.

The amplifier operates from a single positive supply ($V_{DD} = +7v$), a negative supply ($V_{GG} = -2v$) and gain control voltage that ranges from 0v (full gain) to -7v. The operating current is only 325 mA. Compact bias distribution networks are integrated in the form of spiral inductors and MIM capacitors. The only external components required are a single capacitor per bias line. The high level of functionality is illustrated in Figure 3 which shows a comparison between TMM9001 and TGA8722(TI) chip assemblies. The latter circuit is representative of design technology previously available. The new chip requires significantly fewer external components, while providing approximately 10dB greater power and gain. The chip area TGA8722 is 75% that of the TMM9001.

The total gate width in the three stage chip is 2.85 mm. A 0.5 mm input stage drives a 1.0 mm second stage, followed by a 1.35 mm final.

Good power performance was obtained by limiting the number of distributed sections in the output stage to three, in order to provide more uniform power loading. A slight step(taper) to the drain



TMM9001

TGA8722

Fig. 3 Assembly/Bias Complexity Comparison.

line effective impedance is also present. Gate drive voltage uniformity is achieved by series capacitors in the final and an m-derived gate network in the second stage. Single-gate FETs in the third stage also provide a power advantage over a dual-gate FET final.

Simulations were run on S-Compact/Harmonica and Touchstone/Libra. Dual-gate FET were modeled as non-identical cascode single-gate FETs pairs.

Stability has been addressed in several regimes: in/near band (Rollet's) stability margin, UHF stability due to bias de-coupling, and mm-wave stability in dual-gate FET stages. Stable performance has been demonstrated over the full -54C to +90C temperature range by TMM9001 chips processed from over 100 wafers. Mesa resistor and gap capacitor loading of dual-gate drains provides stability at mm-wave frequencies. Feedback in the 0.3-1.0 GHz range through the

bias circuitry was minimized by design (with some resistive loading). Verification of bias circuit effects required a full nodal representation of the entire chip instead of the more typical cascading of stages. Another advantage of this complete representation, is simulation of electrostatic coupling effects between adjacent circuit blocks can be implemented.

COUPLING ANALYSIS

A novel design methodology to account for coupling effects, which become significant in tightly packed chips, has been demonstrated. The technique utilizes a perturbation approach in which a full nodal description of the chip simulates proximity effects using an electrostatic cross-coupling approximation. Figure 4 illustrates the representation of these coupling effects, for a portion of the chip, as discrete capacitors. The method accurately represents coupled microstrip lines of short length by uncoupled lines joined by a coupling capacitor. In this manner, 2 nodes per coupled section are required instead of 4. It is also significant that coupling effects can be represented algebraically for real time optimization. The perturbation approach to circuit coupling has been found to be accurate and computationally efficient.

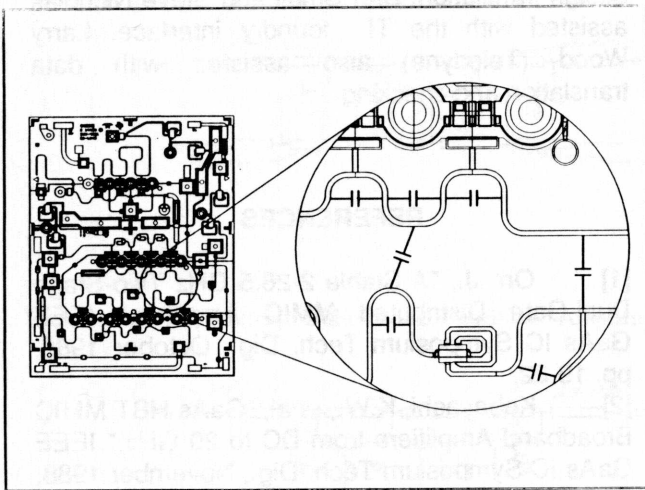


Fig. 4 Parasitic Coupling Representation.

BIAS NETWORK AND GAIN CONTROL

Design features include fully integrated bias networks that provide stable operation over -54 to

+85C and a wide dynamic range of control exceeding 25 dB. The gain control scheme was designed to minimize degradation of output power as gain is turned down. All bias and gain control circuitry are explicitly represented in the net-list.

Variable gain amplifiers controlled by dual-gate FETs can suffer from severe power loss as gain is reduced, due to current starvation. Our approach was to distribute the control over the first two stages, with more gain control effected in the first stage. Additionally, full power performance in the final stage was maintained through fixed bias. Gain control voltage variations are passed through to both gates 1 and 2 of the first stage; but, only to gate 2 of the second stage.

MEASURED PERFORMANCE

A summary of chip RF performance is shown in Figures 5 through 10. The predicted first pass response is in excellent agreement with test results.

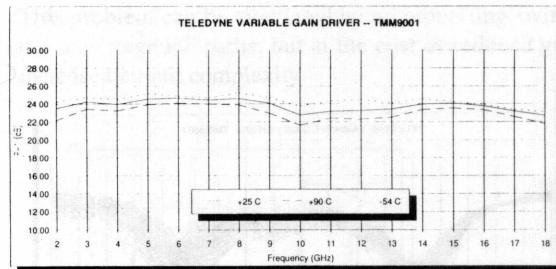


Fig. 5 TMM9001 P-1dB vs Temperature.

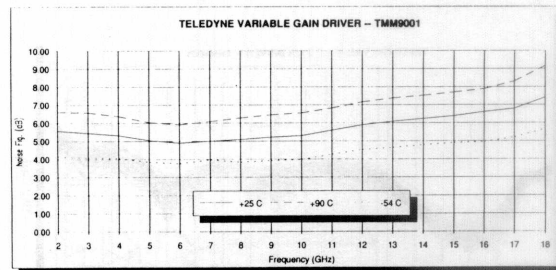


Fig. 6 TMM9001 Noise Fig. vs Temperature.

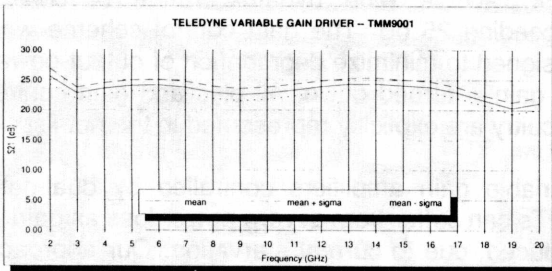


Fig. 7 S21 Statistics, 100 Assemblies.

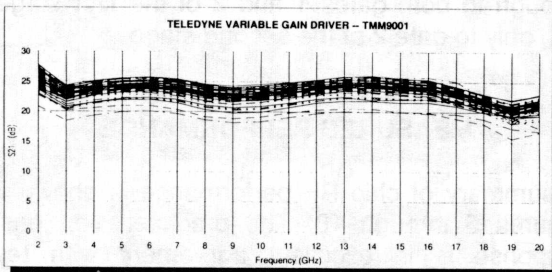


Fig. 8 S21 Cumulative, 100 Assemblies.

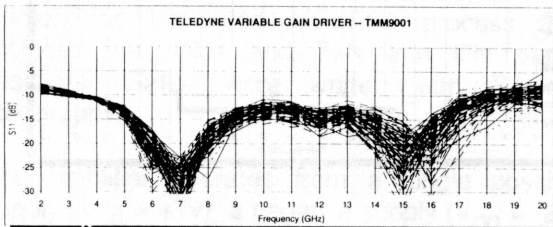


Fig. 9 S11 Cumulative, 100 Assemblies.

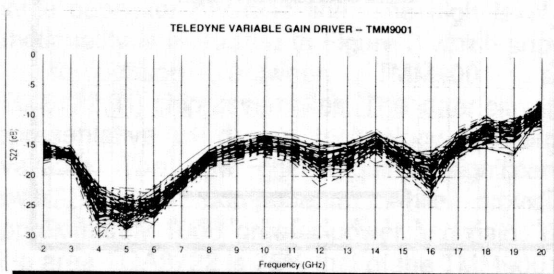


Fig. 10 S22 Cumulative, 100 Assemblies.

Typical small signal gain is +24 dB. Power performance is +23dBm at one dB compression and typical saturated power of +25 dBm. Input and output return loss are typically better than -10 dB. At the optimum noise bias, the noise figure ranges from 4 dB over much of the band to 7.5 dB at the high frequency corner.

CONCLUSIONS

The reported level of circuit density, including integrated bias networks, with typical gains of 24dB and power levels of +23 dBm over decade bandwidth is a significant advance in single chip performance. The demonstrated chip performance highlights the major developments in design technology and foundry process during the past few years, in extending performance capability and repeatability of complex MMIC Circuits.

ACKNOWLEDGEMENT

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